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VOICE OF THE ENGINEER

FEB 2

Issue 3/2006

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DECISION TIME:
CAST YOUR VOTE FOR *EDN*'s 2005 INNOVATION AWARDS
Page 41

FRIEND OR FOE:
BATTERY-AUTHENTICATION ICs SEPARATE THE GOOD GUYS FROM THE BAD
Page 59

DUAL THRESHOLD VOLTAGES AND POWER-GATING DESIGN FLOWS OFFER GOOD RESULTS
Page 65

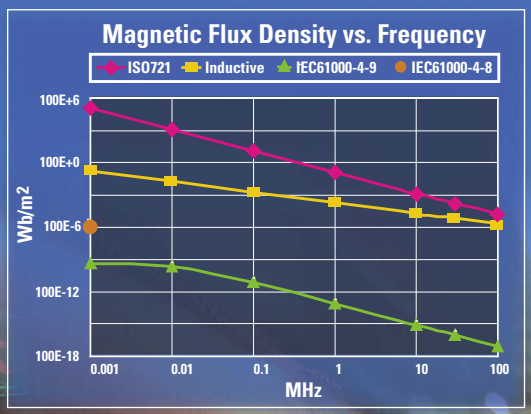
CO-DESIGN

IC AND PACKAGE DESIGNERS SEE EYE TO EYE ON 3-D DESIGN
Page 46

Total Noise Immunity

High Speed, Reliable Capacitive Isolation

TI's capacitive digital isolation technology conveys data across an oxide barrier at significantly higher rates than optocouplers, has substantially improved common mode transient immunity and greatly reduced power requirements. The ISO721 – a highly reliable, single component, EMI resistant solution ideal for your data transmission needs.



High Performance. Analog. Texas Instruments.

For a datasheet, sample and evaluation module, visit
www.ti.com/iso721

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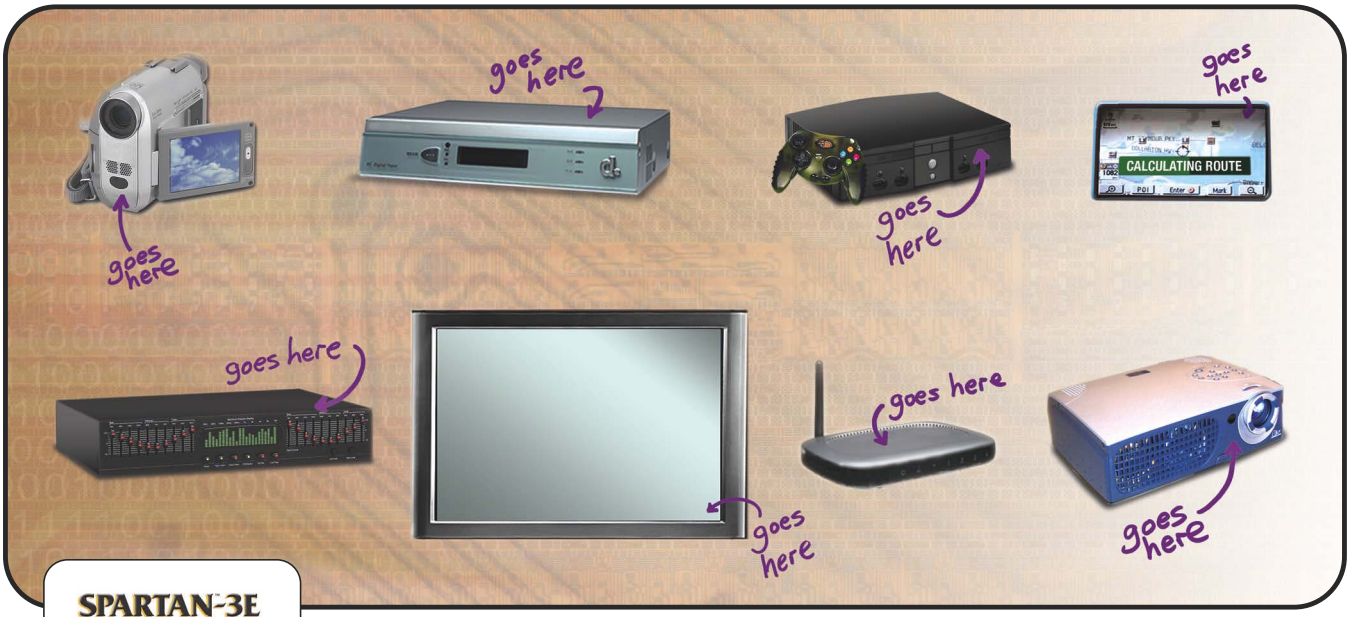
The Spartan-3E family — the world's lowest-cost FPGAs

Priced to go.



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The industry's first 100K gate FPGA for under $2.00*

Spartan-3E Platform FPGAs offer an amazing feature set for just $2.00! You get 100K gates, embedded multipliers for high-performance/low-cost DSP, plenty of RAM, digital clock managers, and all the I/O support you need. All this in production now with a density range up to 1.6 million gates.

Easiest to use Software

Perfect for digital consumer apps and much more!

With the Spartan-3E series, we've reduced the previous unit cost benchmark by over 30%. Optimized for gate-centric designs, and offering the lowest cost per logic cell in the industry, Spartan-3E FPGAs make it easy to replace your ASIC with a more flexible, faster-to-market solution. Compare the value for yourself . . . and get going on your latest design!

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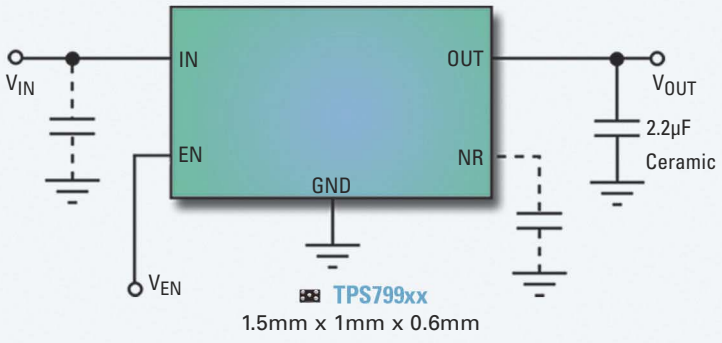
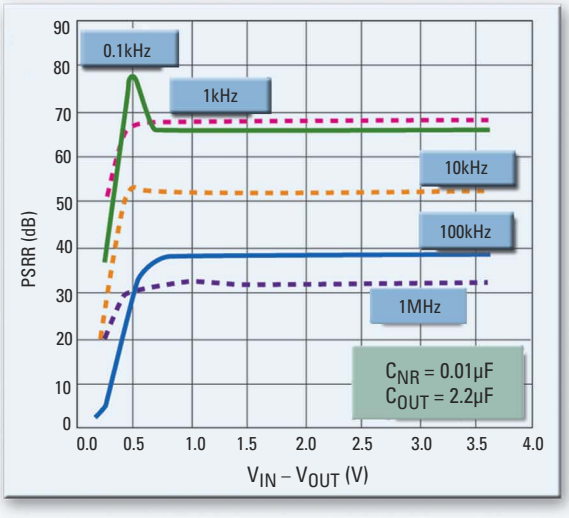
POWER MANAGEMENT

RF LDOs in 1.5mm x 1mm Chip-Scale Package

Single TPS730xx, TPS793xx and TPS799xx



TPS799xx Power-Supply Ripple Rejection vs V_{IN} - V_{OUT}, I_{OUT} = 200mA



▸ Applications

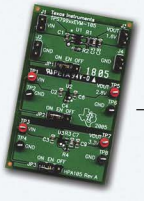
- Smartphones
- Mobile phones
- Digital cameras
- Wireless LANs
- Portable media players

▸ Features

- 1.5mm x 1mm CSP (TPS730xx, TPS799xx and TPS793xx)
- Low noise and high PSRR
- Fast start-up
- Low dropout
- V_{IN} = 2.7V to 5.5V
- Enable pin(s)
- Output current: 200µA
- Ceramic output capacitors
- 1,000 piece price:
  - TPS730xx: $0.25
  - TPS793xx: $0.28
  - TPS799xx: $0.35

Is your design tight on space? The **TPS730xx** and **TPS793xx** ultra-small, single CSP LDOs deliver 200mA per channel. Low noise and high PSRR make these devices ideal for noise-sensitive applications.

For samples and evaluation modules, as well as information on TI's complete line of RF LDOs, visit **www.ti.com/rfldo**



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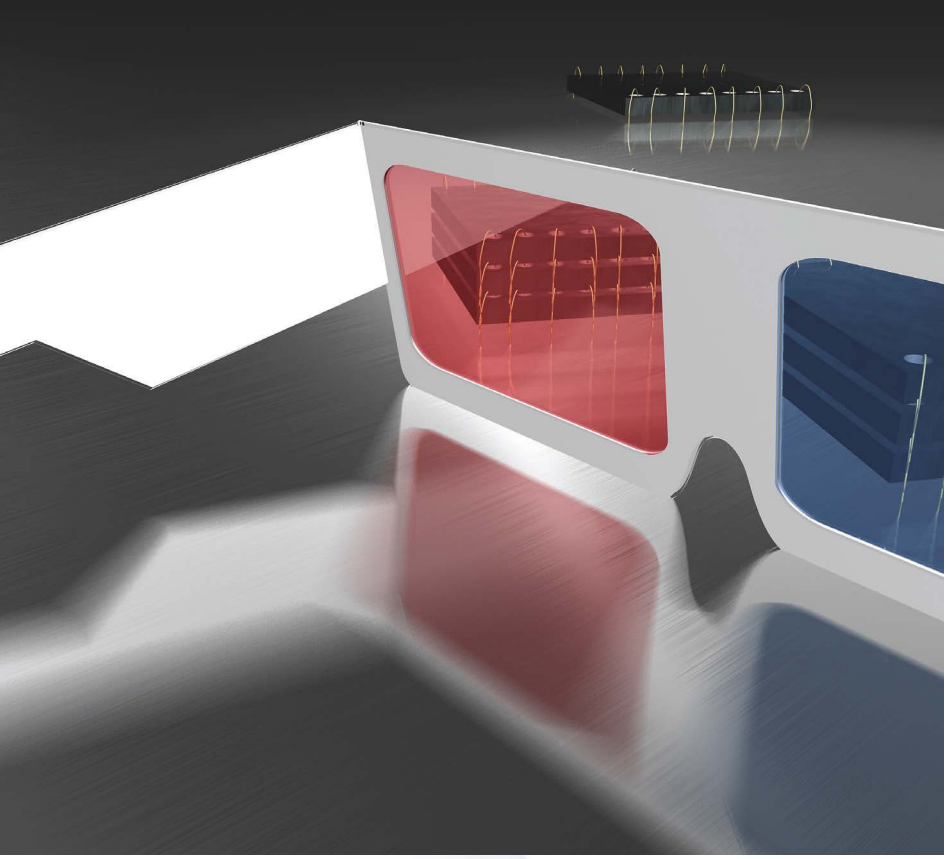


EDN
VOICE OF THE ENGINEER
50 years

contents

2.2.06

Co-design

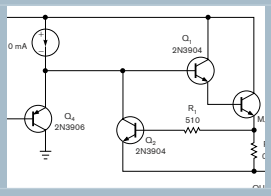
Friend or foe: Battery-authentication ICs separate the good guys from the bad

Decision time: *EDN*'s 2005 Innovator/Innovation Finalists

EDN innovation 16th ANNUAL AWARDS

Dual threshold voltages and power-gating design flows offer good results

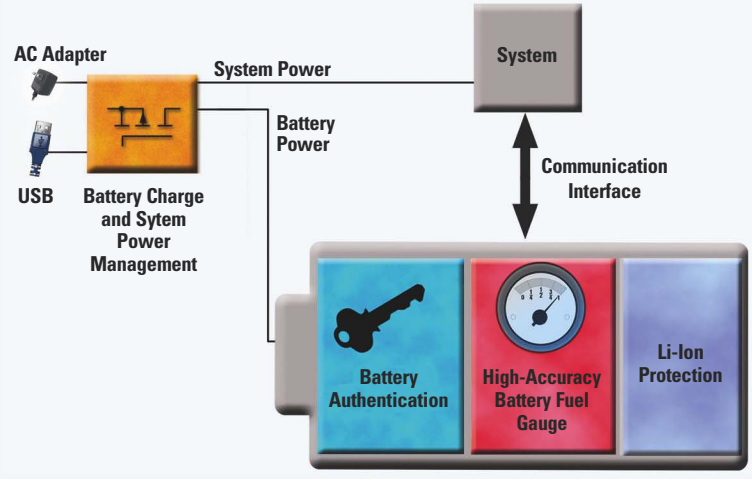
DESIGNIDEAS



▶ Send your Design Ideas to EDNdesignideas@reedbusiness.com.

Battery Management Solutions for Single-Cell Li-Ion

Power Path Management, Charging, Fuel Gauging and Authentication in Handheld Applications



The **bq24030** charge management device integrates dynamic power path management (DPPM), allowing the AC adapter or USB port to simultaneously power the system and charge the battery.

The **bq27000** fuel gauge provides the system all data needed to effectively manage the battery and extend run-time. It requires no calculations by the host microcontroller, resulting in easy implementation of this accurate fuel gauge.

The **bq26150** identifies batteries or accessories that are approved by consumer electronics manufacturers for full performance of their devices. A simple 5-pin device identifies a battery pack via a single-wire bus using an encrypted response to a host-side challenger.

Evaluation Modules available!

▶Applications

- Smartphones
- PDAs
- MP3 players
- Digital cameras
- Handheld devices

▶Features

bq24030

- Power FETs and current sensor, high-accuracy current and voltage regulation, charge status, and charge termination
- Autonomous power source selection (AC adapter or USB)
- AC adapter or USB powers the system directly
- Dynamic charging current based on system requirements

bq27000

- CPU-based IC reports remaining battery capacity, time-to-empty, voltage, current and temperature
- Uses a proven algorithm to adjust calculations for battery characteristics
- Adjusts remaining capacity and run-time prediction for battery inefficiencies

bq26150

- Programmable CRC with a 96-bit unique device ID
- 5-pin, SC-70 package

NEW!
Power Management Selection Guide
Datasheets, Samples, Evaluation Modules and Application Notes

www.ti.com/battman ○ 800.477.8924, ext. Lilon

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contents 2.2.06

pulse

25

38

85

DEPARTMENTS & COLUMNS

PRODUCT ROUNDUP

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Each day, device developers like Robert Bonin are harnessing the power of Microsoft® Windows Embedded to build great devices, like the latest industrial robots from Chaveriat Robotique.

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> ***We chose Windows CE because it offers real-time and graphics at the right price.***
>
> — ROBERT BONIN / **Research & Development Manager** / Chaveriat Robotique / France

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Windows Embedded

EDN online contents

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ONLINE ONLY

Power-miserly audio codec brings fidelity and 3-D sound to portables

The days of lackluster, tinny sounds from cell phones and other portable consumer products may be over with the introduction of Texas Instruments' low-noise TLV320-AIC3x family of 16/20/24/32-bit stereo-audio codecs.

→ www.edn.com/article/CA6300004

Silistix introduces tools to take asynchronous design mainstream

EDA and IP start-up Silistix is unveiling tools that it claims will free IC designers from slavery to a single system clock by allowing them to stitch together IC-design blocks with the company's asynchronous IP bus.

→ www.edn.com/article/CA6299547

Chip enables POE convenience with auxiliary backup

The potential convenience of POE (power over Ethernet) is undeniable. Users can connect devices such as IP (Internet Protocol) phones, remote cameras, or WiFi (wireless-fidelity) access points with no ac adapter. But designers of POE-enabled products must guard against the possibility that an Ethernet link may not support POE or that users have oversubscribed the power budget of a POE-enabled source.

→ www.edn.com/article/CA6299997

Embedded agents to monitor, correct VOIP quality

Texas Instruments today announced an embedded technology that aims to provide distributed, real-time monitoring—and correction—of QOS (quality-of-service) issues on IP (Internet Protocol)-based services, such as VOIP calls.

→ www.edn.com/article/CA6299583

Xilinx confirms acquisition of AccelChip

To grow its market beyond its traditional user base of hardware engineers and tap into the universe of software-savvy DSP designers, Xilinx has officially announced that it has acquired Matlab-to-RTL synthesis-tool-vendor AccelChip.

→ www.edn.com/article/CA6299529

EDN's INNOVATION AWARDS VOTE NOW AT WWW.EDN.COM/INNOVATION

Help *EDN* honor excellence in electronics engineering. The 16th annual *EDN* Innovation Awards program is underway now. *EDN*'s editors have narrowed the nominees down to a group of finalists, which includes outstanding engineers, products, and technologies in 15 categories, and the best contributed articles that appeared in *EDN* in 2005.

Please go to www.edn.com/innovation to get the details on all the finalists, then cast your votes using the online ballot you'll find there.

After we tally your votes, along with votes from our editors and editorial-advisory-board members, we'll announce the winners on April 3 at a gala event in San Jose, CA. (If you'd like to join us, details and tickets are also available at www.edn.com/innovation.) As part of the event, *EDN* will award the Innovator of the Year winner a $10,000 scholarship to donate to the engineering school of his or her choice.

1% AND RATIO-RESISTOR-PAIR PROGRAMS NOW AVAILABLE

In a Dec. 16, 2005, Design Idea entitled "Programs calculate 1% and ratio-resistor pairs," we promised to make two EXE files available for download. However, they did not appear online when they should have. (It's a long story, involving an overzealous corporate virus-scanning system.) We're happy to report the files are available now. Thank you for your patience and interest in these programs. We apologize for the delay.

→ www.edn.com/article/CA6290454

FROM THE VAULT

Articles and extras from the EDN *archives that relate to this issue's contents.*

FRIEND OR FOE: BATTERY-AUTHENTICATION ICs SEPARATE THE GOOD GUYS FROM THE BAD (pg 59):

New battery technologies hold promise, peril for portable-system designers
→ www.edn.com/article/CA6288029

Circuit-protection methods yield more robust products
→ www.edn.com/article/CA514947

CES STARS: TOUGH TO FIND IN MEDIOCRE YEAR (pg 10):

CES daily report: An archive of CES coverage by *EDN* and sister publications *Electronic News* and *Electronic Business*.
→ www.reed-electronics.com/showdailyreport

INITIAL INERTIAL GESTURES (pg 32):

Newton's chips: Low-g accelerometer ICs
→ www.edn.com/article/CA472836

HARDWARE DESIGNER ON AN ELECTRIC CHAIR (pg 38):

Protect your circuits from ESD occurrences
→ www.edn.com/article/CA6283830

Minimize ESD-induced downtime
→ www.edn.com/article/CA509597

BY MAURY WRIGHT, EDITOR IN CHIEF

CES stars: tough to find in mediocre year

I'm sure I missed a lot at the 2006 CES (Consumer Electronics Show). It would be impossible not to at the mammoth show with crowds clogging every aisle—at least in the Las Vegas Convention Center's South Hall and Central Hall. Having just returned, however, I'm convinced that there were simply few highlights at the 2006 rendition. I'd hoped to see major consumer-electronics companies adopt some "no-new-wires" scheme or compromise in the next-generation DVD space. Nada. A coming Black & Decker door lock with a biometric sensor may just have been the best thing there.

Actually, the Blackfin-processor-powered door lock, which Analog Devices showed in its private demo area, wasn't the highlight. But it is likely the first product that I saw that I'll buy. It's due at Home Depot this quarter, presumably at less than $150. You can program the lock, which includes a fingerprint-based sensor hidden under the deadbolt, to admit 100 people. Moreover, you can limit access to specific times to anyone on the list—for instance, a housekeeper.

I missed the Toshiba SED (surface-conduction electron-emitter-display) TV. Every time I got to the booth, there was a huge line to view the TV inside a demo room. I heard that it was spectacular, although it may be spectacularly pricey when it arrives, as well.

I saw a combination PVR/portable-media-player reference design in Philips' private demo area that would be high on my list as a consumer. The Nexperia-processor-powered, high-definition-capable, dual-channel PVR can simultaneously record two programs and store the content on the user's choice of an internal hard disk or a hard disk in a docked portable media player. The user can view the content on the portable player, and the portable player can drive an HDTV, so you can take your high-definition content to visit friends and family. No word on when someone might produce such a product.

Despite boasts by all of the no-new-wires players leading up to CES, no major consumer-electronics company introduced a product with integrated WiFi, UWB, BPL, or data over cable for video distribution.

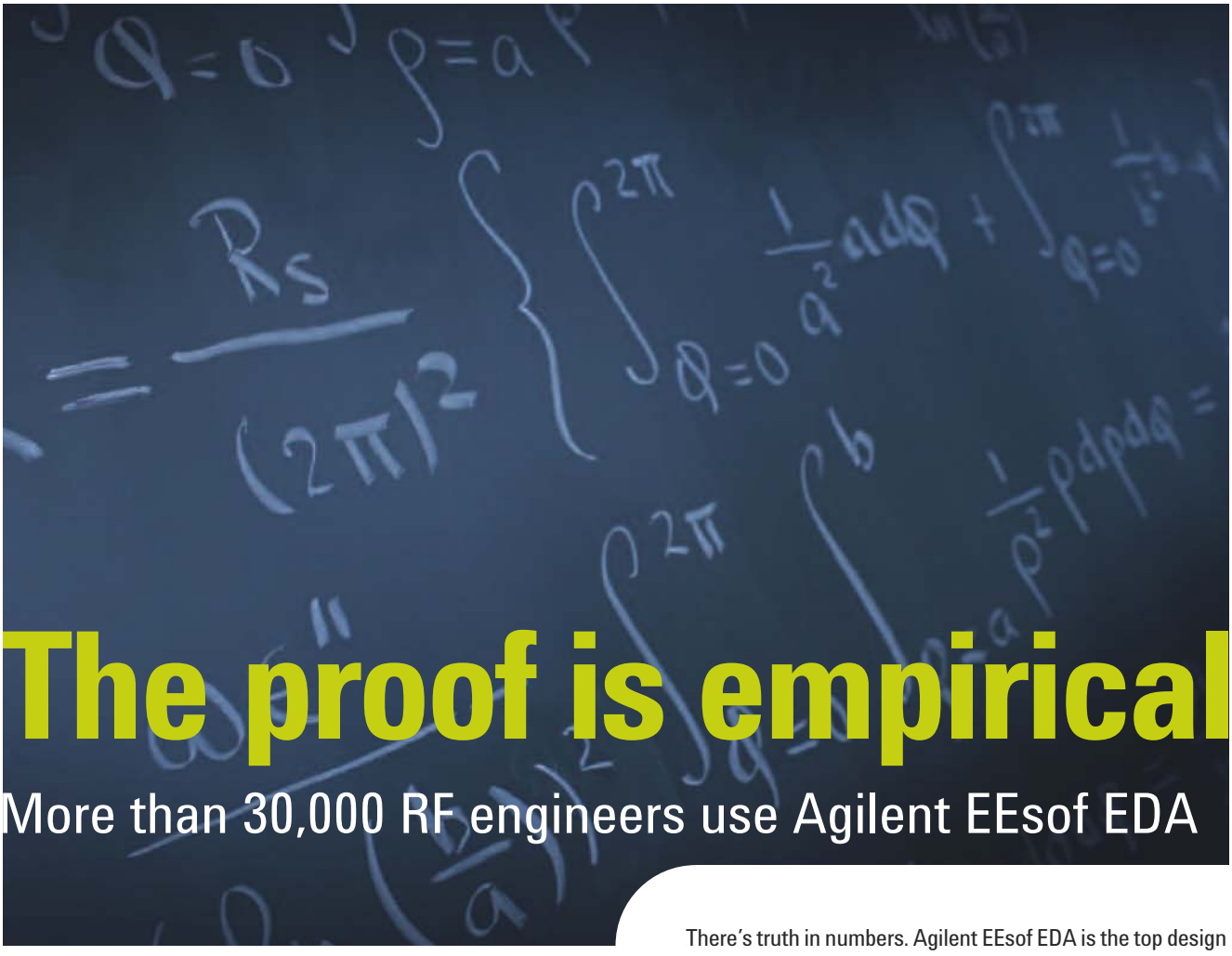
Despite boasts by all of the no-new-wires players leading up to CES, no major consumer-electronics company introduced a product with integrated WiFi, UWB (ultrawideband), BPL (broadband over power line), or data over cable for video distribution. The demos were perhaps a bit more refined than, but largely the same as, those at CES 2005.

The next-generation DVD battle continues to baffle me. Based on products that vendors showed at CES, the early Blu-Ray products will sell for approximately $1500, and the HD-DVD products will come in at less than $500. I realize that Blu-Ray can theoretically store more data, but who cares? Current red-laser-based DVDs can store an HD movie using an MPEG-4-based codec. But Sony continues its pattern of supporting standards only when it can get the industry to adopt its own IP (intellectual property), thereby generating royalties even on products from competitors. To make matters worse, Sony comes up with lame justifications for Blu-Ray, such as insisting that it needs to stick with MPEG-2. This company simply no longer does what's best for the customer.

I've also heard the argument that Blu-Ray is preferable in Hollywood because it will require costly new duplication equipment that will put pirates out of business. It might raise the price of illegal DVDs in Asia to $3, but it won't slow down the pirates. Watch for a comprehensive report on DVD and codec technology from Senior Technical Editor Brian Dipert in early March.

Finally, CES-attendee numbers were about 100,000 short of the 240,000 or so that Comdex claimed in its biggest years. But I don't remember a Comdex with as many people in the aisles and booths. And Comdex never enjoyed the huge space of the relatively new, two-story South Hall. But with such a crowd come complaints. The transportation was a bigger mess than ever. There was no way to leave the convention center in a reasonable amount of time on Friday night. Even the new monorail had a line down the stalled escalator and snaking through the tent village. Gouging in hotel prices hasn't reached the Comdex level, but it's coming close. CES had better learn from the failures of the Comdex organizers. EDN

Contact me at mgwright@edn.com.



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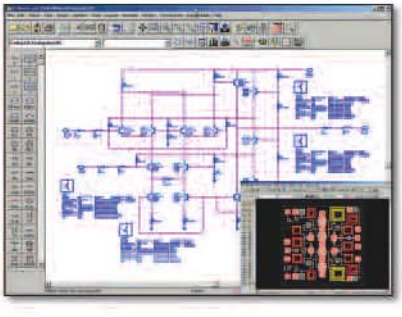

EAGLEWARE ELANIX

Eagleware-Elanix is now part of Agilent EEsof EDA.

There's truth in numbers. Agilent EEsof EDA is the top design software choice among engineers for the vast majority of the world's wireless devices.

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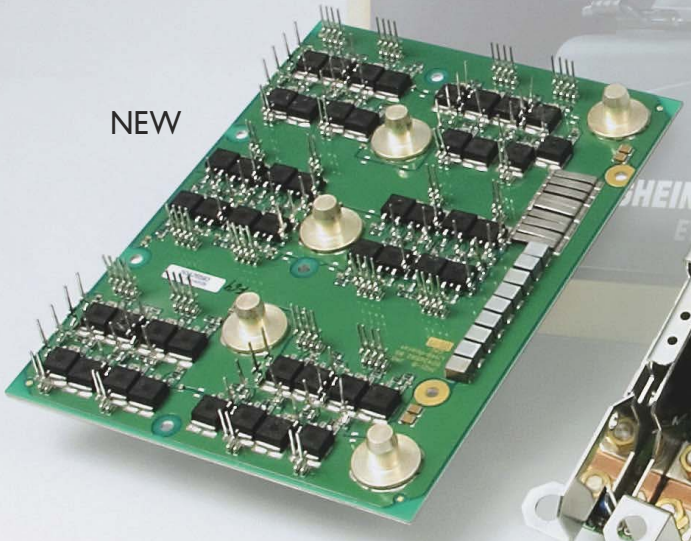
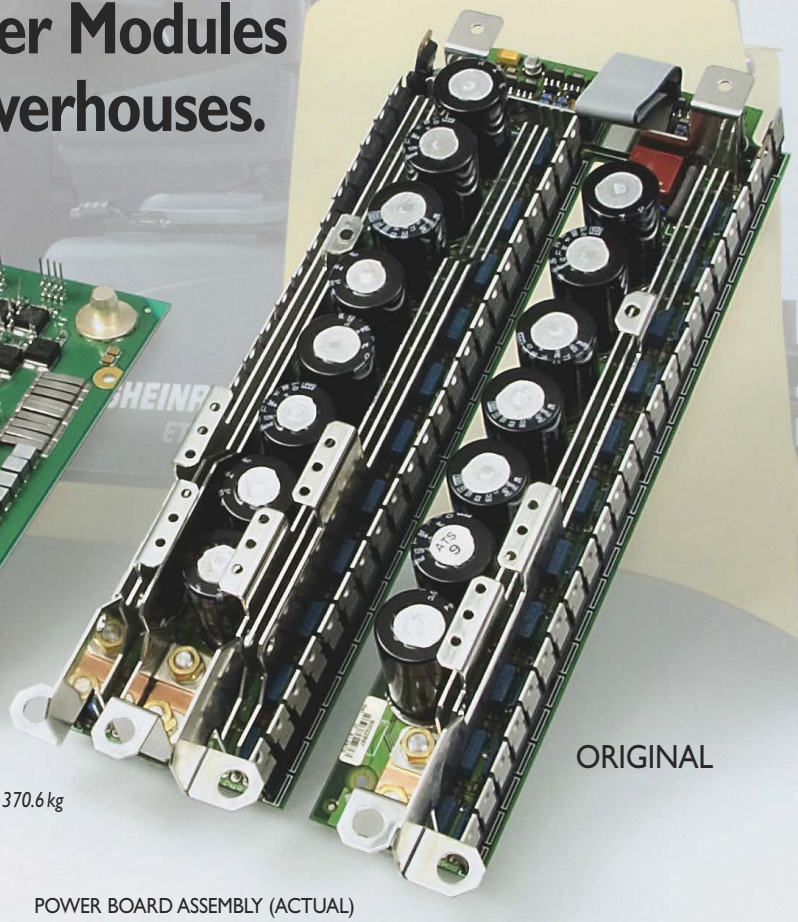
Agilent Technologies

Bergquist Thermal Clad Turns Big Power Modules Into Small Powerhouses.

NEW



POWER BOARD ASSEMBLY (ACTUAL)
(48) FETs (9) Low profile capacitors (5) Low profile bus bars Total Wt. 370.6 kg



ORIGINAL

POWER BOARD ASSEMBLY (ACTUAL)
(66) Thru-hole FETs (15) High profile capacitors (9) High profile bus bars Total Wt. 1543.6 kg

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Stephan Taube
Electronic Development Engineer of Jungheinrich Forklifts

Automated assembly lowers manufacturing costs.

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*i*Polar™: A milestone in high voltage bipolar processing

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By utilizing a proprietary trench isolation technique to enhance NPN/PNP transistor density and functionality, *i*Polar enables dramatically improved performance of linear products with lower noise, smaller packaging, and reduced power consumption. The result? Our new family of 20 V to 36 V bipolar analog products that help increase performance, lower costs, and reduce design time for industrial applications.

And when it comes to supporting the higher voltage needs of industrial customers, that's quite a winning combination.

Lowest noise in the smallest footprint

Our breakthrough manufacturing process yields analog ICs with superior noise and footprint characteristics. For example, the ADA4004-4 precision quad amplifier achieves 1.8 nV/√Hz voltage noise density—the industry's lowest wideband noise in this product category—while its 4 mm × 4 mm, 16-lead LFCSP occupies 70% less PCB area than the competition.

Superior speed and reduced power

*i*Polar technology enables a new generation of components that offer enhanced speed with markedly reduced power consumption. For example, at 10 MHz on 2.5 mA supply current, the AD8675 offers 20% higher bandwidth while consuming 50% less power compared to other high voltage ICs. Likewise, our ultralow offset voltage AD8677 operational amplifier reduces power consumption up to 40% without loss of bandwidth.

Solutions for all your high voltage needs

Our families of high voltage analog ICs are growing. Coming soon will be more *i*Polar devices—such as drivers, voltage references, and additional amplifiers, including new audio ICs. We're also expanding our line of amplifiers, converters, and mixed-signal ICs manufactured on our recently introduced *i*CMOS™ technology. Together these new processes offer state-of-the-art high voltage analog IC performance and value, and represent our ongoing commitment to industrial and instrumentation engineers. For more information, please visit our website.

AD8675
Low noise, rail-to-rail precision amplifier

- Low voltage noise: 2.8 nV/√Hz
- Rail-to-rail output swing
- Input bias current: 2 nA max
- Offset voltage: 75 μV max
- Offset drift: 0.6 μV/°C max
- Very high gain: 120 dB
- 3 mm × 4.9 mm, 8-lead MSOP
- Pricing: $1.17/1k quantities

AD8677
Ultralow offset voltage op amp

- Low offset voltage: 75 μV max
- Input offset drift: 1.2 μV/°C max
- Supply current: 1.2 mA
- High CMMR: 130 dB
- Dual-supply operation: ±5 V to ±15 V
- 2.9 mm × 3 mm, 5-lead TSOT-23
- Pricing: $0.75/1k, quantities

ADA4004-4
Low noise, precision quad amplifier

- Low voltage noise: 1.8 nV/√Hz
- Wide bandwidth: 12 MHz
- Low offset voltage: 100 μV max
- Supply current: 1.7 mA/amp
- Dual-supply operation: ±5 V to ±15 V
- Extended industrial temperature range −40°C to +125°C
- 4 mm × 4 mm, 16-lead LFCSP
- Pricing: $3.02/1k quantities

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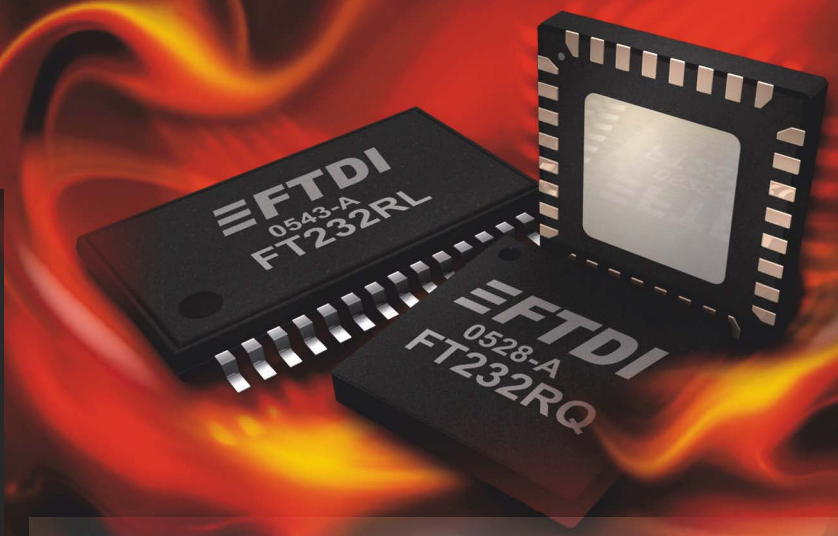
ANALOG DEVICES

FT232R USB UART with MCU Clock Generator and FTDIChip-ID™ Security Dongle



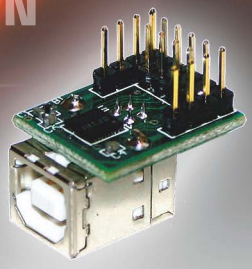
MORE

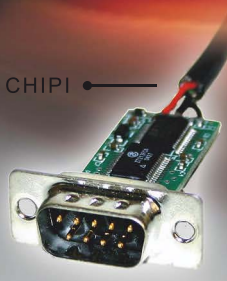
Integration - EEPROM, internal clock generator, and USB termination resistors on-chip.
Functionality - integrates the functions of USB UART, MCU clock generator and Security Dongle into a single chip.
Flexibility - five IO pins can each be user configured as Sleep, Transmit Enable, Power Enable, MCU Clock Output, TX/RX LED Drive or GPIO Pin
Security - FTDIChip-ID™ technology helps protect your application software.
I/O Drive Capability - from 5.5v down to 1.8v levels at 4mA or 12mA programmable strength.
I/O Modes - synchronous and asynchronous Bit-Bang I/O
OS Support - in house developed & supported drivers for Windows 98,ME,2K, Server 2003, XP, XP64, Embedded XP, Mac OS8,9,X, Linux, Win CE + many 3rd party drivers.
Driver Options - VCP and D2XX drivers for all Windows platforms and Linux.
Technical Support - a wide range of evaluation kits available from the outset make evaluating the FT232R a snap.
Package Choices - SSOP28 and QFN32
Interface Options - also available with a parallel FIFO interface
(p/n FT245R).

LESS

External Components - no crystal, EEPROM or USB termination resistors required.
Board Space - new QFN package takes up only 25mm² of pcb area.
Manufacturing Cost - minimal external component count coupled with competitive pricing reduces the overall cost.
Programming - FT232R comes pre-programmed with each part having a unique USB serial number burnt in. This eliminates the need to program the EEPROM in many cases and saves on production time / cost.
Time to Market - FT232R eliminates USB driver and firmware development in most cases thus significantly reducing time to market.

EVALUATION KITS


MM232R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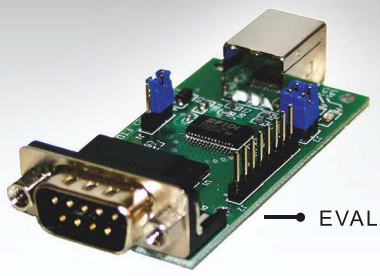
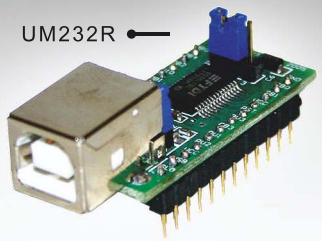
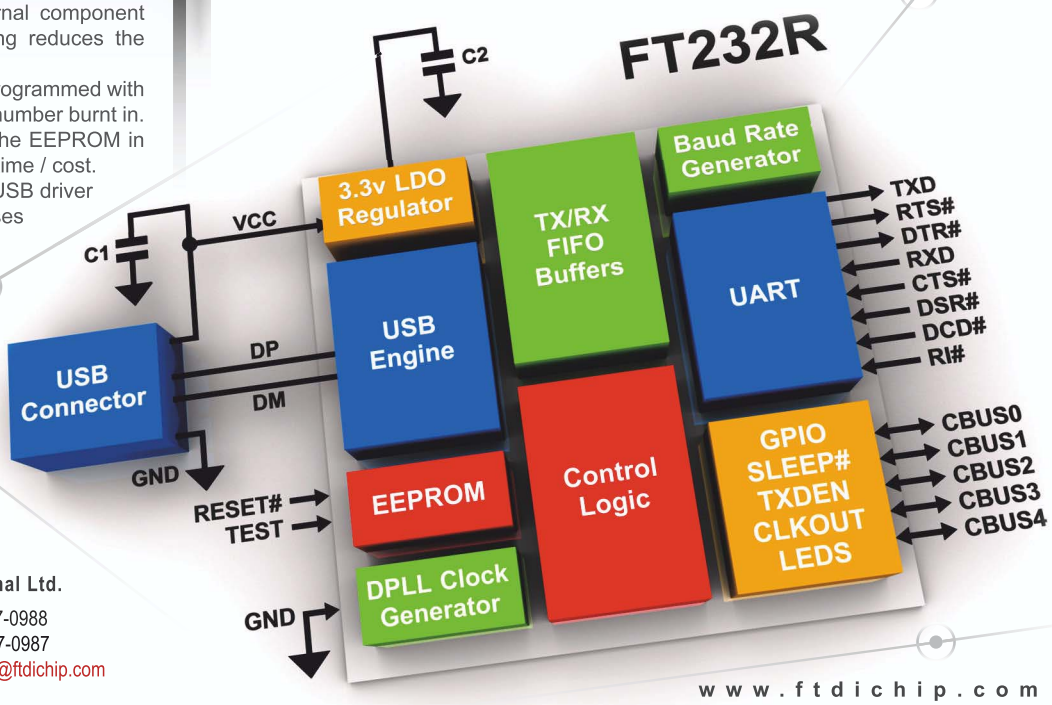

EVAL232R


UM232R

BLOCK DIAGRAM



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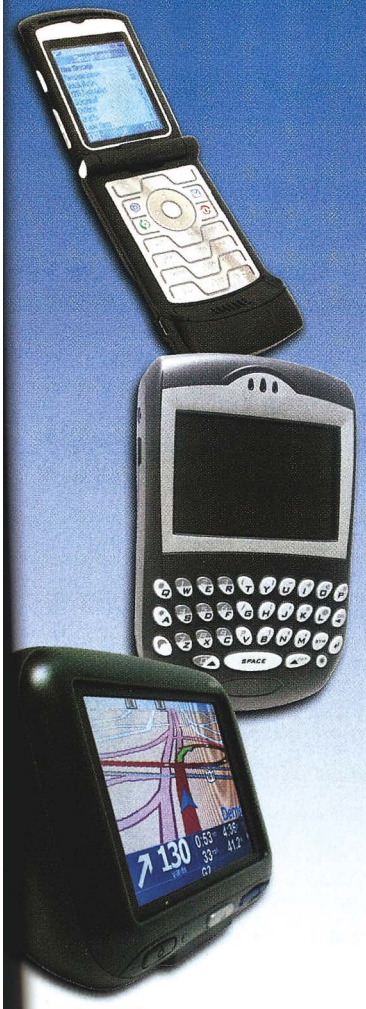


Optimizing RF Power Amplifier System Efficiency Using DC-DC Converters

— By Mathew Jacob, Applications Engineering Manager

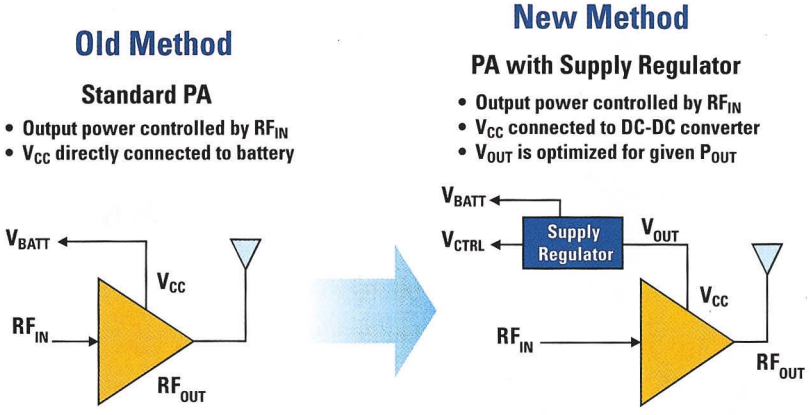


Figure 1. Old Method vs New Method

RF power amplifiers used in CDMA / WCDMA cellular standards have been traditionally powered directly from the battery. This makes system implementation easy but the requirement for linear power amplifiers in such standards have intrinsic inefficiencies throughout the transmit power spectrum.

Cellular standards have been evolving with transmission speeds that started from 14.4 kbps in CDMA-1 to 2 Mbps in CDMA2000/WCDMA. Apart from this, cellular providers have increased the services bundled with the 3G phones in order to increase the average revenue per subscriber. At the same time, the talk time and battery life is expected to be improved with the same or slightly higher capacity batteries. This makes system design challenging. System designers have to be very cautious and perform a power survey of each and every component on the phone board. The RF Power Amplifier (RF PA) powered directly from the battery is a major concern from the power budget perspective.

The modulation schemes used in CDMA and WCDMA result in an amplitude-modulated signal that exhibits a non-constant amplitude envelope. In order to preserve signal integrity and further spectral re-growth, a linear

NEXT ISSUE:

Emulated Current Mode Control

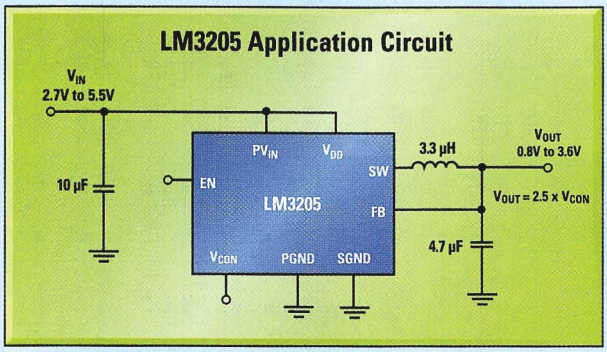
National Semiconductor

Dynamic Power Management of RF Power Amplifiers

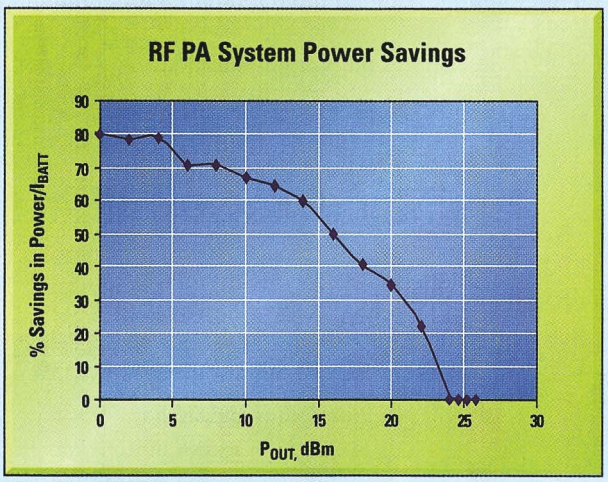
Feature-Rich LM320x Family Enhances Battery Life in Portable Applications

Family Features

- Dynamically adjustable output voltage optimizes RF PA power levels for increased battery life
- Bypass mode maintains maximum output power regardless of battery voltage
- 2 MHz Switching frequency minimizes external components and complies with spectral emission requirements



Ideal for powering RF power amplifiers in cell phones, smart PDA phones, GPS systems, two-way radios, and portable communications systems



Family Highlight:

DC-DC converters deliver up to 5X transmit time in RF PAs

Step-Down Switching Regulators for RF Power Amplifiers

Product ID	Description	V_{IN} Min	V_{IN} Max	V_{OUT}	I_{OUT} (mA)	Bypass Modes	Packaging
LM3200	Dynamically adjustable output voltages, 2.2 µH inductor	2.7	5.5	Adj (0.8 to 3.6V)	500	Forced and automatic	micro SMD-10
LM3202	Miniature, adjustable, step-down DC-DC converter	2.7	5.5	Adj (1.3 to 3.16)	650	None	micro SMD-8
LM3203	Miniature, adjustable, step-down DC-DC converter	2.7	5.5	Adj (0.8 to 3.6)	500	Forced	micro SMD-10
LM3204	Miniature, adjustable, step-down DC-DC converter	2.7	5.5	Adj (0.8 to 3.6)	355/500	Forced and automatic	micro SMD-10
LM3205	Miniature, adjustable, step-down DC-DC converter	2.7	5.5	Adj (0.8 to 3.6)	650	None	micro SMD-8

Optimizing RF Power Amplifier System Efficiency

power amplifier is necessary. However, power efficiency is traded off because power amplifiers operate efficiently when operated in gain compression. To meet the required linearity, the operating transmit power is backed off from the power amplifier's compression point that causes an overall reduction in efficiency. When the handset is operating in transmit mode, the RF power section consumes up to 65% of the overall power budget as a result of the PA's intrinsic inefficiencies.

For this reason, linear PAs are ideal candidates to be powered with a magnetic buck converter which will dramatically increase efficiency of the system.

Power-Added Efficiency (PAE) is a key performance metric of a power amplifier.

$$PAE\ (\%) = (P_{OUT} - P_{IN}) / Pdc$$

The key in using a DC-DC converter (PA supply regulator) is to reduce the Pdc factor in the denominator. When the PA is connected directly to the battery, Pdc=Vbatt*Ibatt and, when it is powered by a PA supply regulator, Pdc=Vo*Io. Now it can be seen that for increasing the PAE we have to have a low Vo and Io compared to Vbatt and Ibatt. This is achieved by lowering the output voltage of the PA supply regulator at lower transmitted RF power levels. This in turn reduces Io (current drawn by the PA) and results in a much lower input current drawn from the battery due to the inherent high efficiency of the DC-DC converter.

It is important to consider the power probability profile (see ***Figure 2***) for the modulation methods to really understand the impact of savings in powering a PA with a supply regulator. The profiles are different for urban and rural regions.

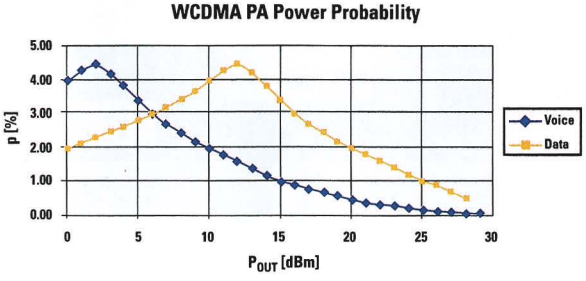


Figure 2. PA transmits low power levels for a high percentage of time in a typical cellular phone which reinforces the savings possible with a PA supply regulator

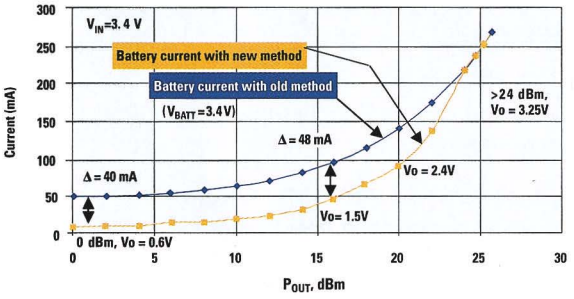


Figure 3. Savings in battery current when the DC-DC converter is used for powering the PA

As shown in ***Figure 3***, the output voltage of the DC-DC converter has to be varied as the transmitted power levels are changed to maintain the Adjacent Channel Power/leakage Ratio (ACPR) specifications. The savings in battery current can be as high as 50 mA in the 0 dBm to 20 dBm power levels. ***Figure 2*** shows that the PA is operating in this band of power levels for a majority of its time.

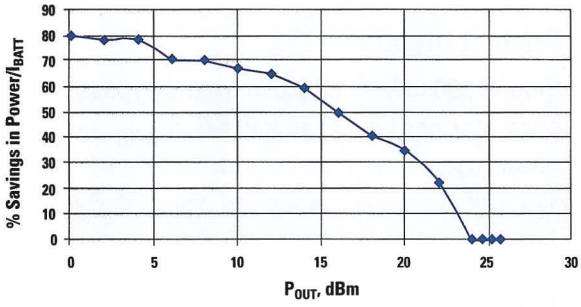


Figure 4. Percentage savings in power when the PA is powered by a PA supply regulator

So why do we have to change the voltage of the DC-DC converter as the transmitted power level is increased? The answer is that this change is needed to maintain the ACPR ratios. ACPR is used to characterize the distortion of power amplifiers and other subsystems for their tendency to cause interference with neighboring radio channels or

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Product Highlight:

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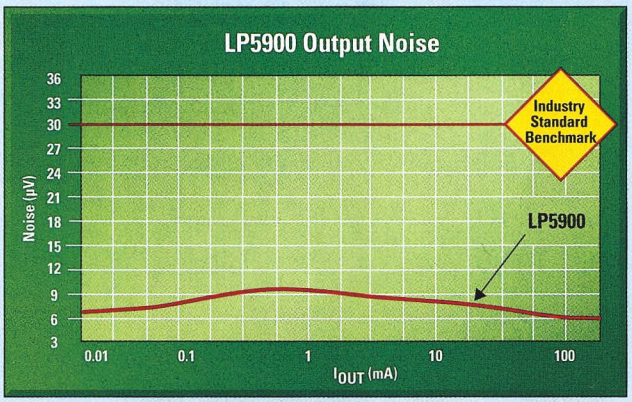
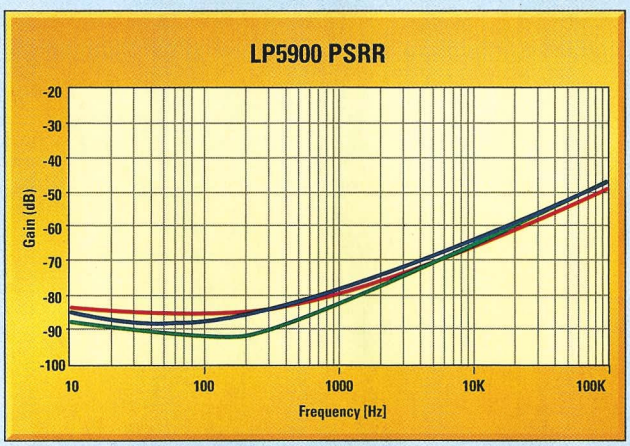
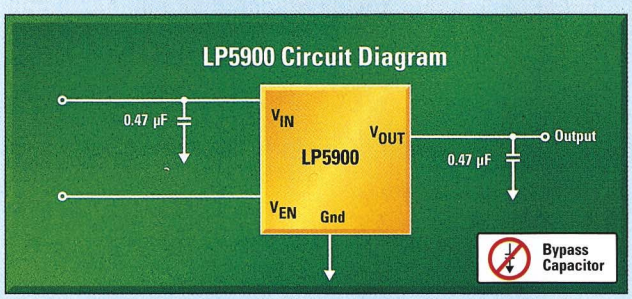






Optimizing RF Power Amplifier System Efficiency

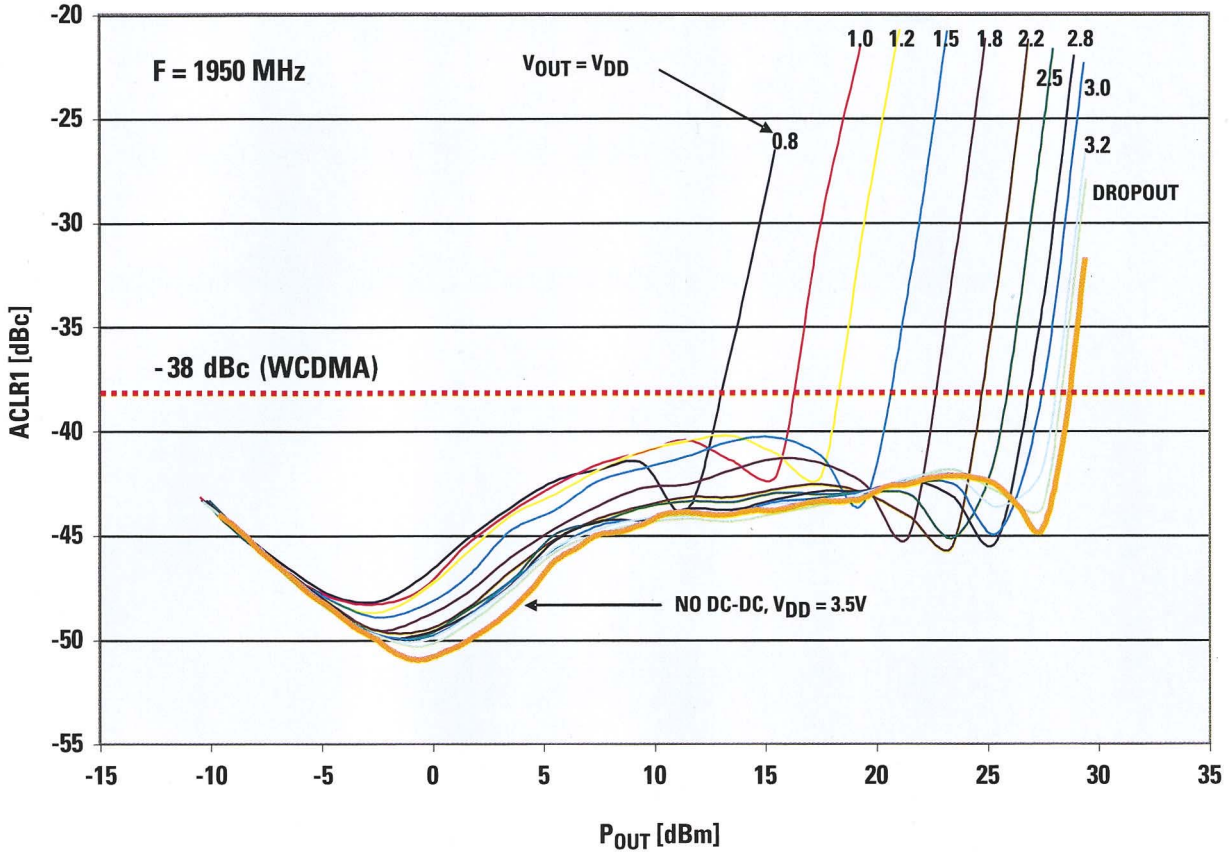


Figure 5. How ACLR is affected with respect to supply voltage to the PA and P_{OUT}

systems. It is specified as the ratio of the Power-Spectral Density (PSD) of the main channel to the PSD measured at several offset frequencies.

In *Figure 5* it can be seen that if the supply voltage to the PA is not increased as P_{OUT} is increased, the ACLR specifications cannot be met.

The system-level specification (3 GPP) for WCDMA is -34 dBc and, in order to preserve sufficient margin caused by temperature and device variances, the ACLR value of -38 dBc is used.

Key Requirements of Buck Converters for Powering RF Power Amplifiers

Buck converters that power RF PAs have specialized functions and are quite different from buck converters that power digital core processors. These differences arise in operating characteristics and parameters such as switching FET ON-resistances, current limit, transient response, modes of operation such as PFM/PWM, startup time, quiescent current, and dropout behavior. The following examples illustrate these differences:

- High efficiency over wide output voltage and load range

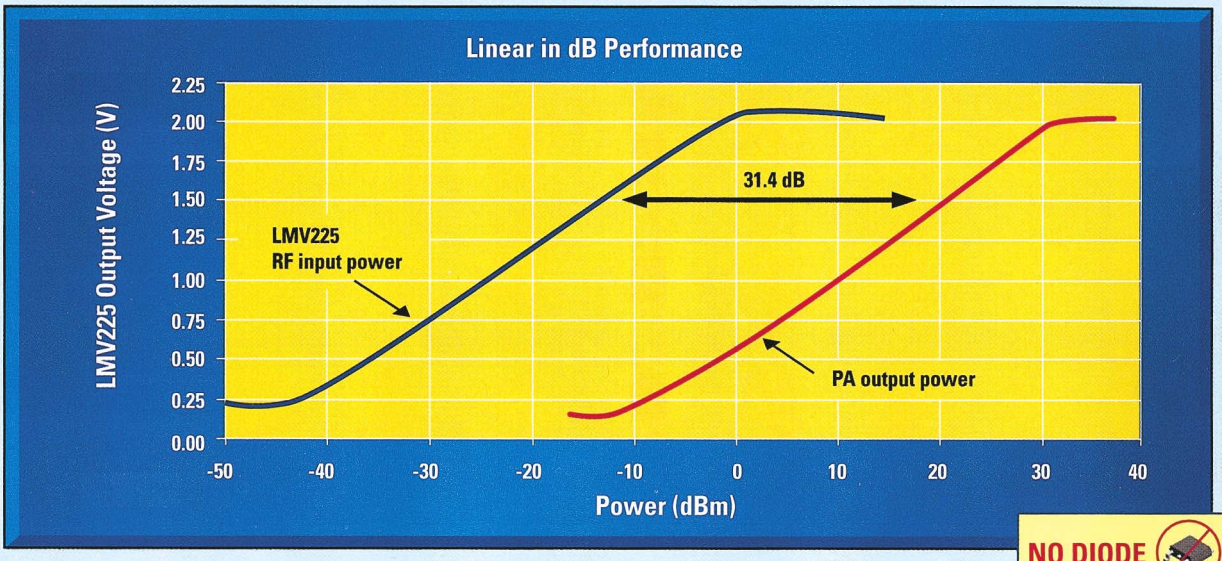
  Example: LM3205 has efficiency of 96% at V_{IN} = 4.2V, Vo = 3.4V, Io = 400 mA (high RF power) and 87% at V_{IN}=3.9V, Vo=1.5V, Io = 100 mA (low RF power).

- Dynamic output voltage adjustment

  Example: In LM3205 the output voltage can be adjusted between 0.8V to 3.6V using a Vcon pin. The voltage gain from Vcon to Vo is 2.5.

Simplify System Calibration with RF Detector Family

Accurate and Stable RF Power Detectors for Portable Devices



Family Features

- LMV227 100% RF tested for accuracy
- 30 dB Linear-in-dB power detection range
- Multi-band operation from 450 MHz to 2 GHz
- Accurate temperature compensation
- Logarithmic amplifier and mean square RF detector technology

Ideal for use in handsets, wireless LAN, WiFi, PC and PDA module cards, and GPS navigation modules

Family Highlight:

Real-time transmitter power adjustments simplify system calibration in communications systems

AVAILABLE LEAD-FREE

Product ID	Application	Detector	Channel	Range	Package
LMV227	CDMA 2000, WCDMA, UMTS	Log amp	1	40 dB, 2.1 GHz	Micro SMD, LLP®
LMV225/226/228	CDMA, WCDMA, UMTS	Log amp	1	40 dB, 2.1 GHz	Micro SMD, LLP
LMV232	3G Mobile communications	Mean square	2	20 dB, 2.2 GHz	Micro SMD

Optimizing RF Power Amplifier System Efficiency

- 30 µs Output slew rate and settling (50 µs window in beginning of every 667 µs transmit cycle in which the Vcon adjustments must be completed) In WCDMA architecture, transmit power is adjusted by ±1 dB in every 667 µs as requested by the basestation.
- Low dropout and low ripple near 100% duty cycle
  Example: Low R_{DSON} PFET 140 mΩ (LM3205) or Bypass FET (LM3204) gives low dropout voltage and pulse-skipping schemes gives low ripple near 100% duty cycle.
- Low duty cycle operation for low output voltages
  Example: Minimum on time, 50 ns facilitates 10% duty cycle operation for output voltages of 0.8V and lower depending on the V_{IN} range.
- High switching frequency
  Example: 2 MHz switching frequency helps the use of smaller sized external components and meet spectral emission requirements.
- Fast turn on time to meet time mask for transmit ON/OFF
  Example: LM3203 has turn-on time of 50 µs for Vo = 3.4V from EN = low to high.

100% Duty Cycle vs Bypass Mode

When the buck converter is operating at 100% duty cycle the dropout voltage is

$$\text{Dropout Voltage} = (R_{ON,P} + R_L) \bullet Io,$$

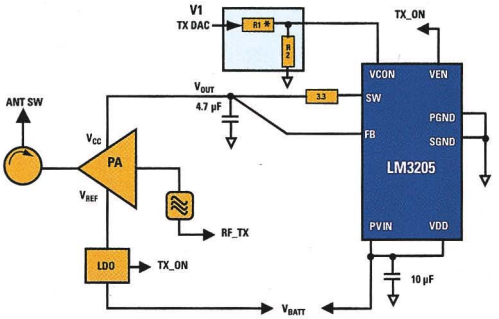
where $R_{ON,P}$ is the R_{DSON} of the PFET and R_L is the inductor DCR. For a PA supply regulator that has a bypass FET the dropout voltage in bypass mode is,

$$\text{Dropout Voltage} = (R_{ON,BYP}) \bullet Io,$$

where $R_{ON,BYP}$ is the R_{DSON} of the bypass FET. The bypass FET can be turned on automatically or manually. As shown, the key advantage in having a bypass mode is lower dropout voltages; which translates to longer talk times and lowering the low battery shutdown point for the phone. The alternative is to use low DCR inductors and a low R_{DSON} PFET.

Example Application Circuits

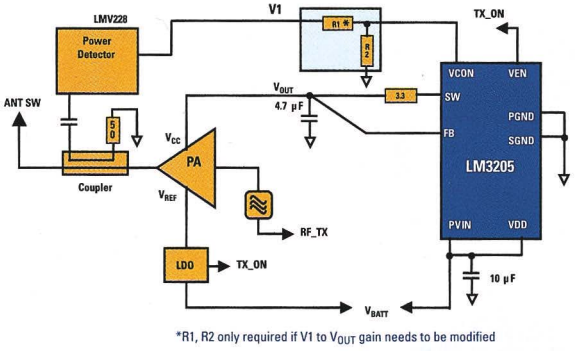
In this example, the baseband will have a lookup table scheme where it sets the output voltage depending on the output power levels required.



*R1, R2 only required if V1 to V_{OUT} gain needs to be modified

Figure 6. Baseband Controls Vo Directly

In this case, the power detector is part of a closed loop and sets the output voltage.



*R1, R2 only required if V1 to V_{OUT} gain needs to be modified

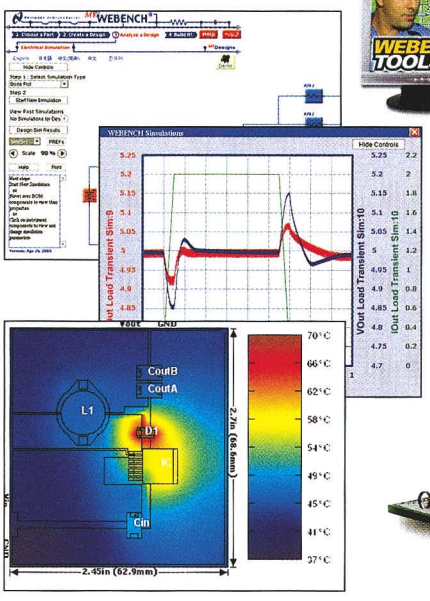
Figure 7. Using a Power Detector to Set Vo

Conclusion

DC-DC converters enhance the RF PA system efficiency in portable communication devices and support the addition of more features or functions by improving battery life. ■

For more information on Powering RF Power Amplifiers, visit www.national.com/onlineseminars to watch Mathew Jacobs' online seminar!

Power Design Tools



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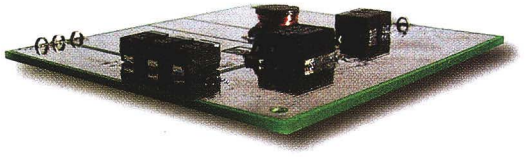

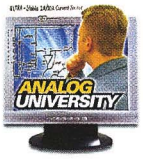

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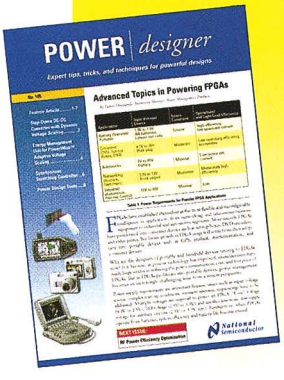

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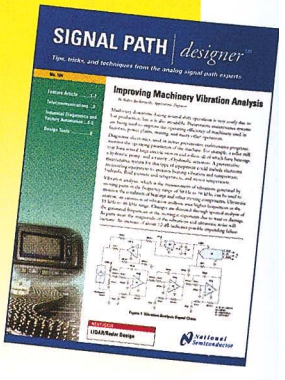

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CANBus, serial networks distribute motion control

Targeting medical, scientific, semiconductor, industrial, robotic, and general-automation applications, Performance Motion Devices recently announced the Ion dc brush drive. This fully enclosed module provides network connectivity, power amplification, and advanced motion-control features for brush, brushless-dc, and microstepping motors in an asynchronous RS485-serial or CANBus-network version. It allows you to connect as many as 127 Ion modules on a network. Ion provides 15A peak output and 500W at 56V.

Other features include hardware-performance trace, on-the-fly profile changes, and PLC-style inputs and outputs. You can program Ion using Pro-Motion, a Windows-based exerciser, or C- and VB-Motion software libraries, which let users develop applications in C/C++ or Visual Basic. Prices for the CE- and ROHS (reduction-of-hazardous-substances)-compliant Ion drive start at $223 (OEM quantities).**—by Warren Webb**

▷**Performance Motion Devices**, www.pmdcorp.com.

The low-cost Ion drive distributed motion controller features CANBus- or serial-port-network connectivity.

16-bit processors get a boost

Microchip is expanding the support for 16-bit processing with the new PIC24 microcontroller family and two new dsPIC33 digital-signal-controller families of devices. These devices deliver more processing performance with more integrated memory and peripherals to lower system costs for 16-bit designs. These devices also support a seamless migration path from Microchip's midrange, 8-bit microcontrollers in nomenclature, pin, and peripheral compatibility. Microchip's universal MPlab integrated-development-environment platform supports software development across the 8- and 16-bit processor families.

The integrated serial-I/O subsystem includes as many as two each of SPI, I^2C, UART, and CAN (controller-area-network) ports. On-chip memory comprises as much as 256 kbytes of flash and as much as 30 kbytes of RAM. The 64- to 100-pin TQFP devices operate at 3.3V. In addition to these features, the general-purpose dsPIC33s include one or two 12-bit, 500k-sample/sec ADCs and a codec interface. The motor-control and power-conversion dsPIC33s differ by offering one or two 10-bit, 1.1M-sample/sec ADCs; a quadrature encoder interface; and PWM for motor-control, lighting, and power-conversion applications. The dsPIC33 devices will become available for general sampling beginning in March and will sell for as low as $5.43 (10,000).

The 16-bit PIC24 microcontrollers debut with 22 general-purpose devices containing as much as 16 kbytes of RAM and 256 kbytes of flash program memory in packages with as many as 100 pins. The PIC24F targets applications that are pushing the envelope of 8-bit-microcontroller capabilities.

Supporting higher processing performance, the 16-bit dsPIC33 in the PIC24 family of devices delivers deterministic execution of as much as 40 MIPS.

The PIC24H delivers more than twice the processing performance of the PIC24F to support more demanding applications, and it includes more memory and additional peripherals, including CAN modules and as many as two 12-bit ADCs. General sampling of these devices will begin in March. The PIC24F is available for prices starting at $4.55 (10,000), and the PIC24H is available for prices starting at $5.16.

—by Robert Cravotta

▷**Microchip**, www.microchip.com.

Networking processors decrease cost, increase integration

Cavium Networks' Octeon CN31XX and CN30XX processors integrate a custom MIPS64 processor core with hardware-acceleration options for layers 3 to 7 data, content processing, and security services at a price as low as $19 (50,000). The hardware accelerators offload the processing requirements from the MIPS core and enable lower system clock rates to achieve gigabit line rates. The new devices offer single- and dual-core devices and are fully software-compatible with the Octeon CN38XX family of multicore processors.

The cnMIPS core implements the MIPS64 Release 2 instruction set with a five-stage, dual-issue, superscalar architecture with a 256-kbyte L2 cache. I/O interfaces include as many as three Gigabit Ethernet interfaces, 32/100 PCI-X, 64-bit DDR2, USB 2.0 host with MAC (media-access-control) and PHY (physical) layers, and TDM/PCM (time-division multiplexing/pulse-code modulation) for voice applications. The CN31XX and CN30XX processors are available as communication processors or secure-communication processors, and the CN31XX processor offers an additional network-services-processor version. The communication-processor version includes hardware acceleration for packet processing, TCP (Transfer Control Protocol), queuing/scheduling, and QOS (quality of service). The secure-communication-processor version adds acceleration for IPsec (Internet Protocol security)/SSL (Secure Sockets Layer), SRTP (Secure Real-Time Transport Protocol), and WLAN (wireless-LAN) security. The network-services-processor version further adds acceleration for deep packet inspection and compression/decompression.

The packet-processing hardware accelerators support L2-L4 packet processing and buffer management for IPv4 (Internet Protocol Version 4) and IPv6 (Version 6) packets. The TCP hardware acceleration includes checks, tag generation, checksums, and timer and buffer management. The queuing/scheduling and QOS hardware implement packet-input queuing/scheduling based on differential services, QOS/TOS (type of service), input ports, or a combination of these features. Cavium based the output-packet queuing and scheduling on a fixed prioritization, weighted fair queuing, or both. The security-hardware acceleration includes full offload for IPsec, SSL, SRTP, and WLAN 802.11i security; it supports DES (Data Encryption Standard)/3DES, AES (Advanced Encryption Standard) as large as 256 bits, AES-GCM (Galois Counter Mode), AES-XCBC (extensions to cipher-block chaining), ARC (Address Resolution Client) 4, MD (Message Digest) 5, SHA (Secure Hash Algorithm)-1, SHA-2 through SHA-512, RSA (Rivest/Shamir/Adleman) to 4096 bits, and Diffie-Hellman. It also includes a true hardware-random-number generator. The compression/decompression hardware acceleration implements GZIP Gnu Zip), PKZIP, and variant protocols. The deep-packet-inspection hardware uses eight pattern-matching engines that perform pattern analysis for intrusion detection, antivirus and content-based switching, routing, and filtering applications.

> Cavium based the output-packet queuing and scheduling on a fixed prioritization, weighted fair queuing, or both.

The CN31XX devices will become available for sampling in the first quarter of 2006 with prices ranging from $49 to $125 (10,000). The CN30XX devices will become available for sampling in the second quarter of 2006 with prices ranging from $19 to $39 (50,000). These devices are available in 525- and 868-pin BGA packages, and they feature power consumption of 4 to 7W. Operating-system support includes Linux, MontaVista Linux, and Wind River (www.windriver.com) VxWorks. A Cavium Networks software-development kit comes with Linux, software examples, a Gnu tool chain, the GDB (Gnu-debugger) development environment, and tool kits for IPsec, SSL, and TCP stacks.

—by Robert Cravotta

▷**Cavium Networks**, www.caviumnetworks.com.

FEEDBACK LOOP

"Been there. When secretly raiding production stock for nonbudgeted lab supplies, one makes do with whatever one can confiscate without getting caught."

Glen Chenier in *EDN*'s Feedback Loop at www.edn.com/article/CA6290456. Add your comments.

DILBERT *By Scott Adams*

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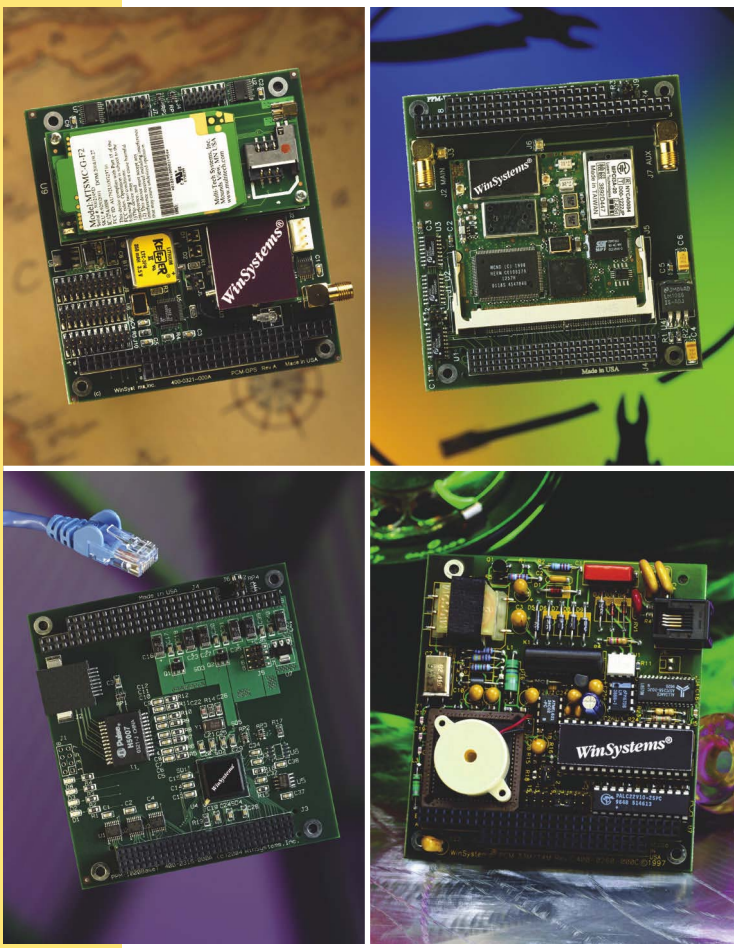

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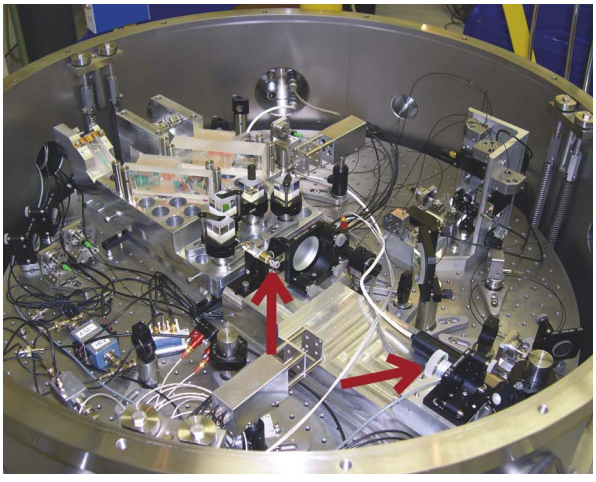


NIST developed an instrument that quantifies millimeter-range distances with accuracy akin to measuring the distance between New York and Los Angeles within 1 mm.

RESEARCH UPDATE

BY MATTHEW MILLER

Scientists boast about their small measurements

In separate work, researchers at NASA's Jet Propulsion Laboratory and the NIST (National Institute of Standards and Technology) have developed new laser-based methods for measuring distance with mind-boggling precision. The NASA scientists designed a laser-based heterodyne interferometer that can precisely measure a range as great as 100 km with resolution of 1 nm. The MSTAR (modulation-sideband technology for absolute range) relies on multiple wavelengths generated as sidebands of phase modulation of the light from a single laser. See www.nasatech.com/Briefs/Nov05/NPO_30304.html for details.

NIST, meanwhile, reported the development of a technique that can measure millimeter distances with uncertainty of 10 pm. The technology, which focuses on measuring the frequency, rather than the wavelength, of the light, could have applications in nanotechnology, remote sensing, and semiconductor fabrication. See www.nist.gov/public_affairs/techbeat/tb2005_120105.htm for more details.

▷**NASA Jet Propulsion Laboratory**, www.jpl.nasa.gov.

▷**National Institute of Standards and Technology**, www.nist.gov.

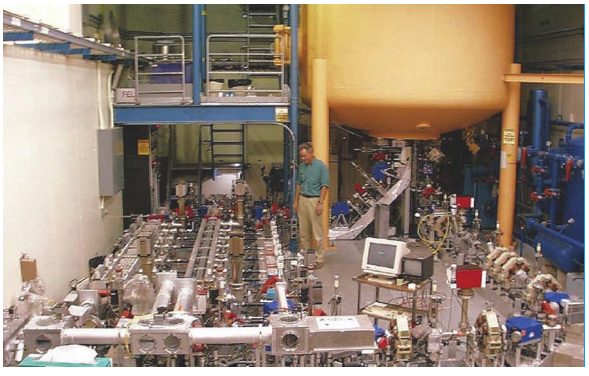
Optical modulator heralds terabit/sec data rates

Researchers at the Georgia Institute of Technology claim to have operated an optical modulator at terahertz frequencies, an advance that may eventually lead to data communications that scientists can measure in terabits (trillions of bits) per second. Traditional optical modulators use a voltage change to alter the reflectivity of a material, which in turn varies the intensity of a light beam passing through the material. But such modulators face a speed limit: They can operate no faster than the electronic circuitry that drives the voltage change.

So, instead of electronics, the Georgia Tech group employed very-high-frequency electromagnetic waves generated by a free-electron laser to modulate the light signal. The researchers state that much work remains before commercialization will be possible.

Chief among the challenges that engineers face is the need to develop power-conscious, inexpensive sources of electromagnetic energy that are considerably smaller than the free-electron-laser facility that the research effort uses.

▷**Georgia Institute of Technology**, www.gatech.edu.



Engineers need to develop power-conscious, inexpensive sources of electromagnetic energy that are smaller than the free-electron-laser facility that the researchers use.

If these walls could heat—and cool

02.02.06

In homes of the future, walls and windows coated with an invisible layer of micrometer-scale photovoltaic cells and thermoelectric materials will provide heating and cooling far more efficiently than traditional systems. At least that's the hope of researchers at the Rensselaer Polytechnic Institute, who are working to develop the technology under a $300,000 National Science Foundation grant. The research aims to scale down the ABE (active-building envelope), which uses exterior solar panels to generate electricity for one-in-two heat pumps dispersed inside a building's walls, windows, and roof. The group hopes that thin-film materials will enable engineers to embed similar functions in a coating material less than 500 microns thick, which, unlike with the ABE system, they could apply to existing construction.

▶**Rensselaer Polytechnic Institute,** www.rpi.edu.

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TI's first DaVinci products offer "easy video"

Texas Instruments has fleshed out the details of the first deliverables under the DaVinci brand, highly integrated product offerings for digital-video designs. DaVinci bundles silicon and software with development support that will allow you to build video products without expertise in codecs or DSP. It allows you to design with video building blocks at a higher level of abstraction than writing and assembling all of the code. This release includes two chips, plus multimedia (software) codecs, API (application-programming interfaces), frameworks, and development tools. The devices let you add digital video to an application with no more involvement than writing to an API, although you can also use the offering as a gateway to the more detailed capabilities of Code Composer Studio.

The TMS320DM6443 handles video decoding, and the TMS320DM6446 decodes and encodes. They integrate a C64 DSP core with an ARM 926 core, plus video accelerators, networking peripherals, and memory interfaces. Capabilities include analog- and digital-video output with resizing and an on-screen-display engine. The 6446 has a front-end capture unit that handles multiple video formats.

In its first release, TI bases the software platform on Linux, with MontaVista (www.mvista.com) as the development-tool provider. To this support, the software part of the offering adds open APIs, device drivers, and multimedia codecs. TI hints that it will offer other operating systems in a future release. The company emphasizes that the silicon in this announcement is an enabling component and presents the overall release as a digital-video-system offering; in hardware, however, it's also worth noting that TI equipped the chips to directly connect to a wide range of analog peripherals that it has chosen not to integrate.

At the development level, you work entirely in the Linux environment, with middleware hiding the details of the codecs. Similarly, interprocessor communications between DSP and RISC engines are also parts of the package. However, programmers who wish to work in Code Composer Studio will be able to exercise control over the ARM core from that package. In operation, you call DSP functions through the ARM. This method, TI says, allows a modular, building-block approach to application design. You can exchange a software codec for an upgrade or alternative or scale an application up or down. A fully equipped digital-video-evaluation module, including a camera, supports the introduction.

–by Graham Prophet, *EDN Europe*

▷**Texas Instruments**, www.ti.com.

FEEDBACK LOOP

"The wire must be obtained, procured, scrounged, begged, borrowed, or just plain stolen at midnight from a production department that has stock in only one color: green."

Glen Chenier in *EDN*'s Feedback Loop at www.edn.com/article/CA6290456. Add your comments.

OS steps up to support proliferating multicore CPUs

02.02.06

In recognition of the rapidly growing interest in multicore-processor designs, QNX has introduced a multicore edition of its development tools. The company asserts that the structure of its operating-system software lends itself to multicore processing and enables it to offer support for all multiprocessing models. The package combines existing products with some changes to the OS kernel. With the software, you can migrate code to a multiprocessor environment. QNX supports both asymmetric and symmetric models. Multiple OS instances–not necessarily the same OS–run on the asymmetric model; each runs on a physical processor. The operating systems fully manage resources. QNX notes that interrupts need special care in this respect. In symmetric processing, a single instance of the OS runs on multiple CPU cores. You can progressively migrate applications, initially allocating tasks to CPU cores and then later moving to a symmetric-multiprocessing model.

You can also use a "bound-multiprocessing" mode, in which you allocate critical tasks and threads or tasks written for single-core operation that you do not wish to rewrite to a given processor. The software can perform controlled- or dynamic-load balancing around this type of allocation at runtime. Multicore technology is coming, and not just for power reasons, QNX says. The company is also finding applications in mobile systems in which having multiple cores running at lower clock speeds yields a better overall power budget.–by Graham Prophet, *EDN Europe*

▶**QNX**, www.qnx.com.

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ANALOG DEVICES

BY JOSHUA ISRAELSOHN, CONTRIBUTING TECHNICAL EDITOR

Initial inertial gestures

As much as micromachined accelerometers enabled new applications for inertial sensors nearly two decades ago, it's been packaging innovations for MEMS (microelectromechanical-systems) devices that have multiplied those opportunities manyfold. This statement is not to suggest that the back-end process developments alone could have created the large emerging markets for MEMS inertial sensors but rather that the opportunities for inertial sensing had early on been somewhat hamstrung by limitations imposed by the packaging available at the time. Today's chip-scale MEMS-packaging technologies offer excellent angular alignment—on the order of ±1°—and fit three-axis devices in substantially smaller footprints than previous-generation single-axis sensors.

Among the most commonly touted new applications are free-fall detectors for disk drives in laptops and other portable equipment and gesture-based user interfaces for mobile phones. The demands such applications make on sensor performance are not necessarily obvious, and, from a systems-design perspective, they suggest that sensing-subsystem designers should carefully construct the rules that govern how the sensor interface interprets its source signal early in the development cycle. The laptop-drop detector, for example, could try to account for all six degrees of freedom—translation in x, y, and z axes and rotation in roll, pitch, and yaw—to calculate the instantaneous inertial state and, in so doing, determine a state of free fall. More simply, it could determine that any shift from the nominal state greater than, say, 0.5 to 0.7G along any axis is sufficient evidence of an *event of interest* to park the drive heads. The distinction is that of threshold detection versus measurement.

Significant advances in user-machine interfaces invariably migrate from early-adopting applications to a much broader range of OEM products.

The end concern with free-fall detection obviously does not center on the free-fall event per se; it's not the fall, as the old joke goes, but the sudden stop at the bottom against which the system must guard itself. So the challenge is not to measure the instantaneous inertial state with precision but to quickly and *sufficiently* assess the inertial state to determine whether action is necessary.

Gesture inputs impose a more complex set of operating conditions and detection goals and, though they do not mitigate destructive events, once promised they are no less critical to customer satisfaction. Unlike a laptop computer, the orientation of which changes little over a brief period during normal operation, a mobile phone's orientation during use is arbitrary and subject to rapid change. Additionally, it is unlikely that parking a drive's heads for a short time while a laptop's orientation is changing would diminish the user's experience, but ending a mobile telephone call, for example, by confusing the normal range of user motion for the control gesture meaning *hang up* is unacceptable.

Mobiles must also accommodate a comparatively large number of operating modes, each of which requires its own set of control inputs. On-hook functions, dialing, call-in-progress functions, and the phone's ancillary subsystems, such as a camera or an MP3 player, all invite their own combination of common and unique gesture in puts. The fact that the handset could be simultaneously executing multiple functions only complicates further the design of gesture-interpretation hardware and software.

Admittedly, few of us design laptops or mobile phones; one could question the relevance of this line of thinking to the design tasks that engage us. Yet significant advances in user-machine interfaces—rare though they may be—invariably migrate from early-adopting applications to a much broader range of OEM products. Few traditional user-interface designs need to consider end-user-behavior variability to the extent that gesture-based interfaces do, and we can learn much by watching how the pioneers, who exploit these interface technologies early, address the challenges. EDN

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Joshua Israelsohn is Director, Technical Information at International Rectifier Corp and is a contributing technical editor at EDN *Worldwide. His engineering experience includes work on MEMS accelerometers and gyroscopes.*

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ANALOG DEVICES

BY BONNIE BAKER

Frequency-domain analysis helps with delta-sigma

I usually look at ADCs in the time domain. When I do, I can determine at least the basics, such as the length of the input-signal sampling time as well as the elapsed time before the data arrives at the digital outputs. This approach usually yields enough information to understand the fundamentals of how to use the converter. Once I understand the converter-timing basics, I can go even deeper.

For instance, I can trace the internal timing operation of the modulator on the delta-sigma ADC using the diagram in **Figure 1a**. The input of the difference amplifier subtracts the DAC output from the input signal. The input of the integrator then sees the resulting voltage at the output of the difference amplifier (V_1). The output of the integrator (V_2) ramps positively or negatively with time. As the voltage at V_2 goes from high to low or low to high across V_{REF}, the comparator switches accordingly (V_3). The system clock of the delta-sigma ADC latches the output of the comparator into the DAC and decimation filter. The combination of the output of the comparator and the system clock also creates a 1-bit stream to the decimation filter. The decimation filter usually has an internal FIR (finite-impulse response) or IIR (infinite-impulse response). In **Figure 1**, the decimation-filter model is a simple averaging filter. The ADC system clock determines the throughput timing of the decimation stage.

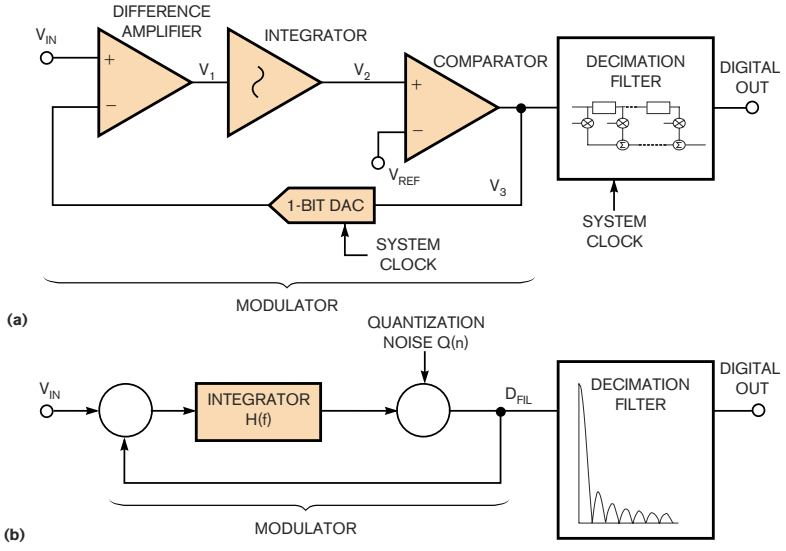

Figure 1 I can model a first-order delta-sigma ADC in the time domain (a) or the frequency domain (b).

Figure 1b shows a frequency-domain model of a delta-sigma ADC. The transfer function for this model from the input signal (V_{IN}) to the input of the decimation filter (D_{FIL}) is equal to $D_{FIL}=Q(n)/(1+H(f))$. The comparator in **Figure 1a** acts as a 1-bit ADC with a quantization error of $\pm 1/2$ LSB, while generating random white noise across the full frequency spectrum (Q(n) in **Figure 1b**). In the transfer function, the open-loop gain of the integrator reduces the quantization noise at low frequencies, pushing the unwanted noise out into higher frequencies. The spectral characteristics of the decimation filter digitally allow lower frequency signals to pass and attenuate the unwanted high-frequency noise.

The time-analysis model can provide a nuts-and-bolts understanding of the delta-sigma ADC (**Figure 1a**). It demonstrates the mechanics of the conversion of the input voltage to output data over time, which is important to know when I use the converter. It also lets me analyze how the digital filter effectively increases the ADC resolution. But the nuance I miss in **Figure 1a** is the effect of the modulator's filtering over frequency. With the model in **Figure 1b**, the impact on the noise of the modulator over frequency is quickly visible. The model in **Figure 1a** provides insight into how to use the converter. The model in **Figure 1b** tells me why the delta-sigma converter is superior for high-resolution applications. EDN

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Bonnie Baker is the author of A Baker's Dozen: Real Analog Solutions for Digital Designers. *You can reach her at Bbaker1632@aol.com.*

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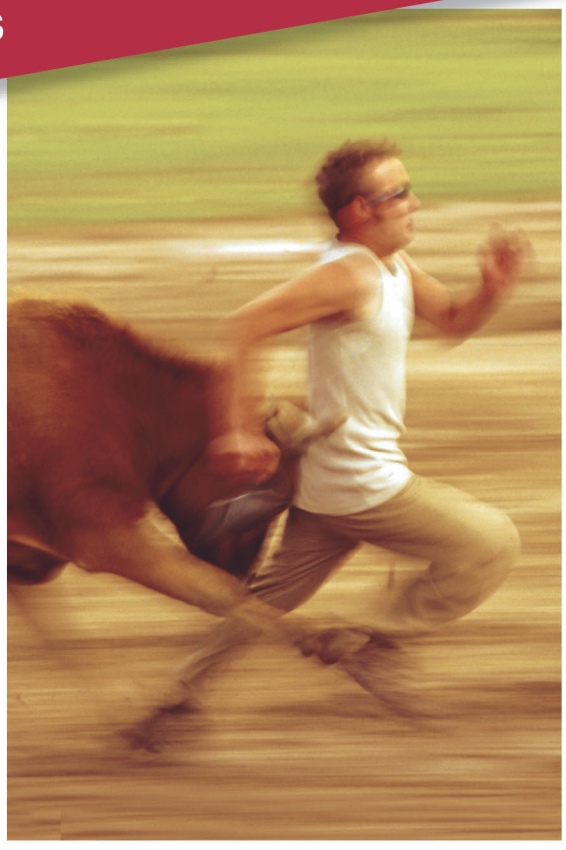

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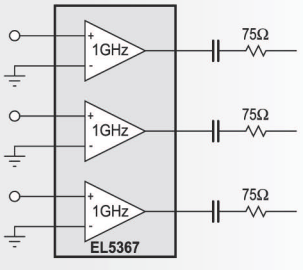

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EL5160/1	1	200	1700	0.75	1	70	±3.4	5
EL5162/3	1	500	4000	1.5	1	100	±3.6	5
EL5164/5	1	600	4700	3.5	1	140	±3.8	3.5
EL5166/7	1	1400	6000	8.5	1	160	±3.8	5
EL5260/1	2	200	2000	0.75	1	70	±3.4	5
EL5262/3	2	500	2500	1.5	1	100	±3.6	5
EL5462	4	500	2500	1.5	1	100	±3.6	5

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Part No.	# of Amps	BW (MHz)	SR (V/µs)	VN (nV/√ Hz)	Is (mA)	IOUT (mA)	VOUT (V)	VOS (max) (V)
EL5100/1	1	300	2200	10	2.6	100	±3.4	5
EL5102/3	1	400	2200	6	5.2	150	±3.7	5
EL5104/5	1	700	4500	14	9.5	160	±3.8	5
EL5202/3	2	400	2200	6	5.2	150	±3.9	5
EL5204/5	2	700	3000	10	9.5	160	±3.8	10
EL5300	3	200	2200	10	2.5	100	±3.4	4
EL5302	3	400	2200	6	5.2	150	±3.7	5
EL5304	3	700	3000	10	9.5	160	±3.8	10

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BY HOWARD JOHNSON, PhD

Specsmanship

Every Joe at the lumberyard understands that a 2×4 does not measure 2 in. by 4 in. Those "nominal dimensions" may apply at the rough-cut stage, but the actual finished dimensions are approximately 1.5×3.5 in. after air drying, planing, and rounding the corners so you don't get splinters. If you need an accurate, straight piece of wood, then after kiln drying, you must pass your stick through a second joiner/planer phase. This operation shaves off even more wood, leaving perfectly square, true surfaces on all four sides with no bow or twist.

What about knots? Good lumber carries a grading stamp related to the severity *and location* of knots and other imperfections. Grading is tricky. For example, a beam held horizontally takes most of its stress near the top edge (compression) and bottom edge (tension), leaving the middle region relatively stress-free. A big knot in the middle of a board, therefore, may not degrade the rating. If you cut that same beam in half lengthwise so the big knot appears on the side of the new structure, where stress is highest, the rating plummets.

Architects and builders understand these issues. They call out the specific type and grade of lumber for every part of a new building, such as "green Douglas fir, grade standard or better." They also design in a substantial margin of safety to account for the reality of manufacturing in their industry—sloppy assembly, inability to read or follow directions, and materials a grade or two below the called-for specifications.

Similar considerations affect electronics. A 5V capacitor doesn't last long when you use it at 5V. A 16-bit ADC doesn't really provide 2^{16} equally spaced quantization levels. A 150-Gbyte disk doesn't really hold 150 Gbytes. Engineers must take these issues into account. In that way, the electronics industry bears a certain similarity to the lumber business.

Little prevents a manufacturer from supplying a nominal model claiming one level of performance but delivering something quite different.

However, one important difference exists. Every year, electronic-component manufacturers spew forth nominal specifications, typical operating parameters, and models "indicative of nominal performance but not guaranteed." Engineers then use these models, verbatim, in simulators all over the world, to verify the correctness of their designs. *Where is the safety factor?*

In other words, suppose an engineer uses 2×4 models that measure 2 in. by 4 in. He assumes every board runs straight and true, with no knots, and then proceeds to design things using this model. He makes no allowance for error. Are you laughing yet?

Seriously, there are no rating agencies for semiconductor models, no federal regulations, and no safety inspectors. Little prevents a manufacturer from supplying a nominal model claiming one level of performance but delivering something quite different.

For this reason, designers of military, medical, and high-reliability equipment always derate component specifications. They account for extremes of power-supply fluctuation, ambient temperature, loss of active cooling systems, material variation, memory errors due to high-energy particle radiation, and the expected degree of specsmanship on the part of their component suppliers. Then, if they really want the product to work, designers test all components before putting them into the system.

Not every project deserves such scrutiny, but, if you do not allocate a healthy margin of safety in your simulations, you deserve a good knock on the head with a nominally dimensioned 1.5×3.5-in. piece of green Douglas fir, standard and better grade. EDN

MORE AT EDN.COM

Go to www.edn.com/060202hj and click on Feedback Loop to post a comment on this column.

Howard Johnson, PhD, of Signal Consulting, frequently conducts technical workshops for digital engineers at Oxford University and other sites worldwide. Visit his Web site at www.sigcon.com or e-mail him at howie03@sigcon.com.

Intersil Battery Charger ICs

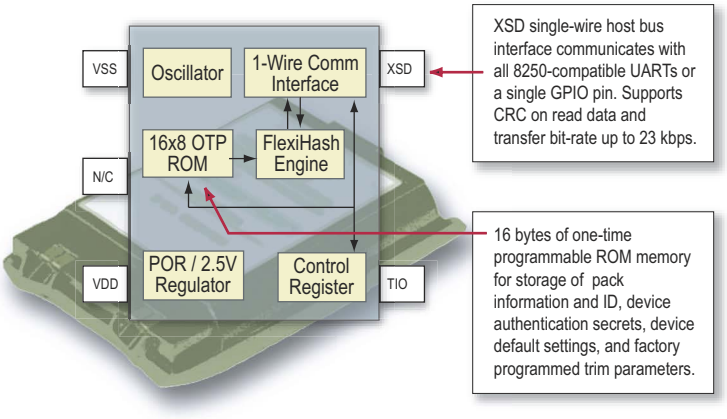
Intersil High Performance Analog

Don't Get Burned by Cheap Imposters

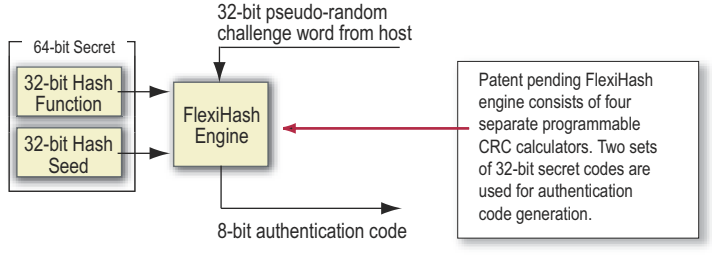
Protect your designs from counterfeit battery packs with Intersil's ISL6296. We've integrated our FlexiHash™ technology to deliver a simple, robust and inexpensive battery authentication solution for 1-cell Li-Ion/Li-Polymer or 3-cell NiMH series battery packs.

Intersil's ISL6296 offers the same level of effectiveness as other significantly more expensive, high maintenance, monetary-grade hash algorithm and authentication schemes. This device supports a wide range of operating voltages and is customized for low-cost applications.

ISL6296 Functional Block Diagram



Device Authentication Process



Key Features:

- Patent pending challenge-response authentication scheme using 32-bit challenge code word and 8-bit authentication code.
- Fast single-step authentication process
- Supports 1-cell Li-Ion/Li-Polymer and 3-cell series NiMH battery packs (2.6V-to-4.8V operation)
- Compatible for use with serial ports offered by all 8250-compatible UARTs or a single GPIO pin
- "Zero Power" sleep mode after bus inactivity time-out period
- 64-bit user-programmable secret for security
- Can also be used in a variety of accessories such as printer ink cartridges where authenticity needs to be verified.
- Variety of packages available including SOT-23-5, chip scale or unpackaged die

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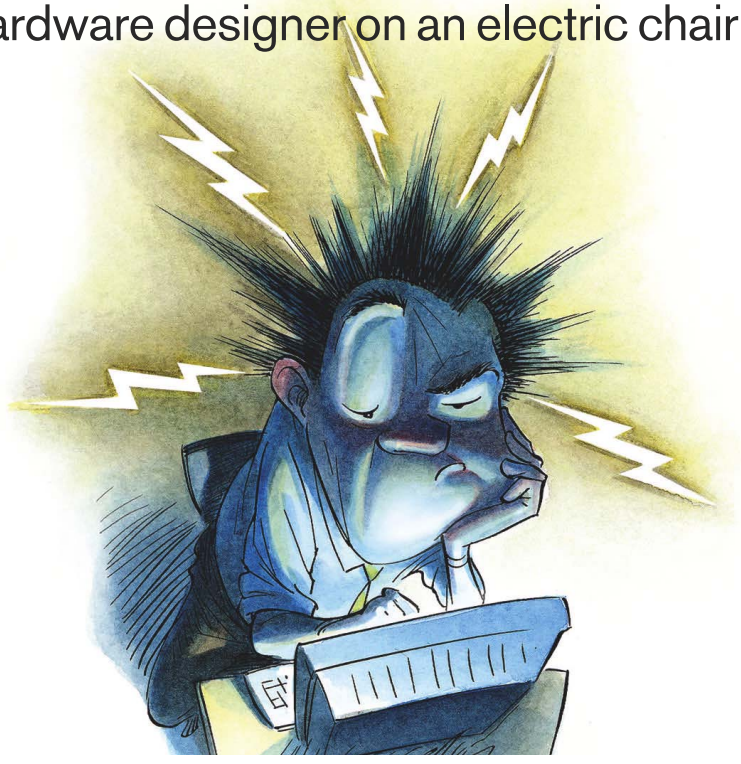
Hardware designer on an electric chair



DANIEL VASCONCELLOS

My engineering team was designing a signal-processing board for the mobile-radio infrastructure. The board integrates a number of DSPs and ASICs for number-crunching. Our team works on both hardware and software development, because experience has shown that this is the most efficient way to deal with such a complex project. The hardware designers sit near colleagues who write the software that runs on the card. Especially in the prototype phase, they work hand in hand. And the physical location sometimes generates unexpected interference.

The early software release—which we optimistically called the "beta version"—must run on the first "alpha board." Even the tiniest error in one of the parts can lead to severe and false accusation. These accusations can often split the team. Nevertheless, we came along that early prototype phase without losing friends on the other side of the hardware/software divide.

About a year into the design, we observed sporadic errors on a high-speed ASIC-DSP interface. The probable cause could be a coding error in the complex DSP software, which would be easy to fix but hard to find in the 1000 lines of code, or a design error in the proprietary ASIC. If the design error were the cause, we would need to build a new ASIC mask, busting the budget and causing a nightmare for our project. The software developers traced the error to an interface access that terminated unexpectedly. But they could not get any deeper into the board.

So, the software side called us on the hardware side for help. We packed our 20G-sample/sec digital real-time oscilloscope with 3.5-GHz probes and moved to the software designer's desk. Our mission was to have a careful look at the critical interface-control lines. The software colleague ran his sophisticated code, while we waited for the error to occur on the oscilloscope screen. Mysterious spikes—with immense amplitudes of about 2V—appeared every now and then on the control lines. Could the spikes be the reason for the sporadic interface failure? Where did they come from? We spent several hours changing interface-timing parameters, recompiling the software, measuring, and changing the parameters again with no luck.

We were frustrated and tired, looking hopelessly at the screen exactly when the oscilloscope triggered. Then, I saw a colleague getting up from his chair and leaving. That was it! The ESD (electrostatic discharge) he generated by getting up caused an amplitude of several volts, even over a distance of several meters.

In our hardware lab, we wear ESD-protective shoes, sit on special ESD-protective chairs, and walk on ESD-reducing flooring. The software lab had no such ESD protection; it was a typical office on which software designers in rubber-soled shoes walk on a synthetic carpet or sit on standard office chairs. In an office with 10 engineers, someone was always moving on a chair, getting up, or sitting down. The movement was causing the sporadic, mysterious spikes. After that revelation, we reproduced the setup in our hardware lab. In the following days, we finally traced the board failure to a software bug in the DSP.

Several months later, an intern observed a similar effect when working with an evaluation board. After two hours of catching mysterious spikes on the scope, he called me for help. He was obviously anxious. Although he was using all the ESD-protection features in our lab, he feared having killed either the high-speed scope probes or the chip-evaluation board. But, within two minutes, we found the culprit: the grounding wire connecting the back of his chair to the base. It was broken. After fixing the wire, the problem disappeared, and we have never seen any of the mysterious spikes again. **EDN**

Thomas Blinn works for Siemens (Ulm, Germany), where he has realized the importance of staying on an antistatic mat.

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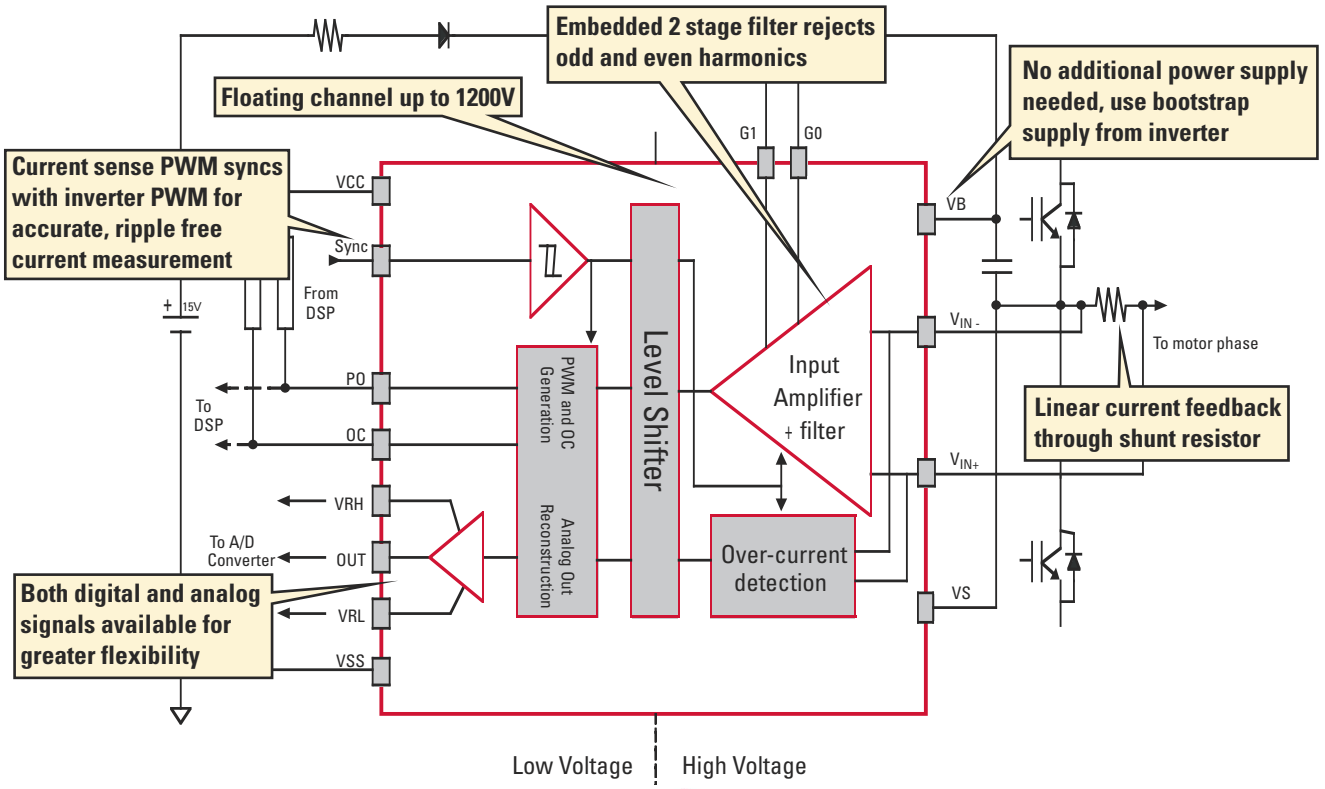

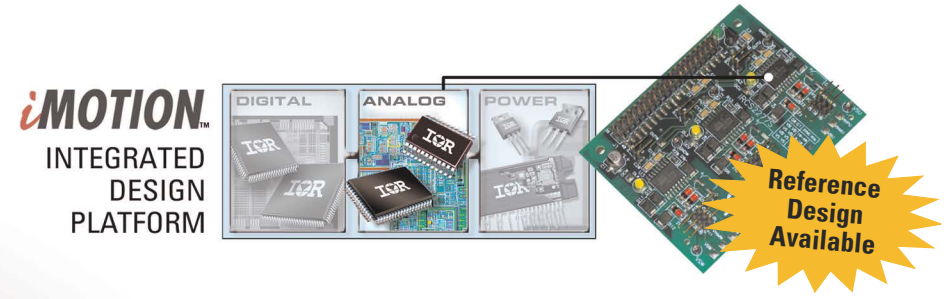

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V_{IN} range	+/-260mV	+/-250mV	+/-250mV
Carrier output frequency bandwidth	15kHz	20kHz	20kHz
Over-current threshold	+/-260mV	+/-470mV	+/-470mV
Analog output dynamically adjustable	N/A	Yes	Yes
Package	8-pin SOIC	16-pin SOIC	16-pin SOIC
2-Stage filter	No	Yes	Yes
Bootstrap supply range	13-20V	8-20V	8-20V
External sync	No	Yes	Yes

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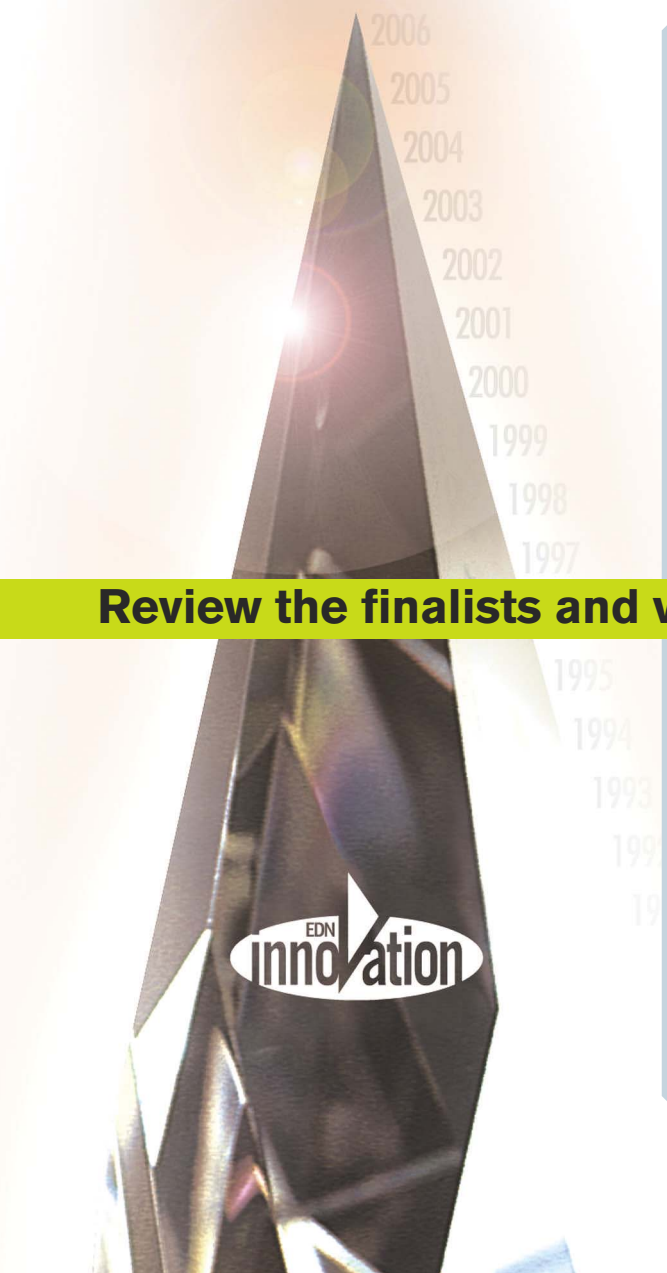

People in this industry throw the word "innovation" around a lot. Most of the press releases that come to *EDN* claim to bear news of an innovation, usually one that's "groundbreaking" or "revolutionary." But the marketing department does not define true innovation. The engineers who strive to achieve it day after day are the ones who define it because they're the people who understand what it really takes to create something that breaks new ground.

No one's better equipped to recognize true innovation than you. So, our editors have gone so far as to choose a group of finalists for *EDN*'s 2005 Innovation Awards. But we need your help picking the winners. On the following pages, we'll introduce you to the finalists, including outstanding engineers, products, and technologies in 15 categories and the best contributed articles that appeared in *EDN* in 2005.

Review the finalists and vote at www.edn.com/innovation.

Please go to www.edn.com/innovation for details on all of the finalists and then cast your votes using the online ballot you'll find there. We'll honor the winners April 3 in San Jose, CA. (If you'd like to join us, you can also find event information and tickets at www.edn.com/innovation.)

Thank you for helping us to honor the work that you do.

EDN's 2005 Innovation Finalists

INNOVATOR FINALIST VIP50 process team, National Semiconductor

Designing an innovative, high-performance IC is one thing. Creating an entirely novel process technology to support the creation of any number of innovative, high-performance ICs is quite another. National Semiconductor's VIP50 team, encompassing six geographically dispersed groups, labored for more than two years to develop the industry's first SOI (silicon-on-insulator) BiCMOS analog process for amplifier applications.

Combining efficient, bipolar transistors; analog-grade MOS transistors; highly matched, low-temperature-coefficient thin-film resistors; and laser-trim capability, the VIP50 process is allowing the company to spin out precision and low-power, low-voltage op amps that deliver dramatically better performance than their predecessors. For example, the LMV651, which the company introduced in September 2005, provides a tenfold improvement in speed-to-power ratio compared with other offerings and reduces power consumption by 90%.

The team (of which only a fraction appears in the photograph) successfully tackled a number of complex challenges, including optimizing the high-speed, vertical NPN and PNP bipolar transistors to work well with less-than-1-μA operating currents; tweaking the technology's MOS transistors for good matching behavior and low 1/f-noise characteristics; and developing new test and packaging technologies.

EDN *nominates VIP50 as an Innovation in the Analog ICs category.*

INNOVATOR FINALIST EinsTimer statistical-timing development team, IBM Research

Corner-based timing is painting IC designers into a corner, but the EinsTimer team crafted a potential means of escape. The traditional static approach to ASIC timing closure, based on "corner," or "case," files, focuses on designing for worst-case scenarios. This pessimistic method leaves much-needed performance on the table. Worse, static tools are proving unable to comprehend the random—and potentially showstopping—process variations that are becoming more numerous and severe as geometries shrink.

With EinsTimer statistical timing, a parameterized, block-based statistical timer, the IBM team (some of whom appear in the photo) proved that statistical timing can be both accurate enough and fast enough for multimillion-gate designs. To do so, the team had to take on and surmount challenges including variational gate and wire modeling, statistical calculations, correlations, software architecture, and incremental timing. The resulting tool reduces pessimism, provides efficient process coverage, and demonstrates the viability of concepts that will become even more important as the design process itself becomes more probabilistic.

In addition, the team's innovations extended beyond the technical aspects of the project and into the development process itself. For example, the team implemented new ideas directly on a production platform, thus avoiding the customary prototype phase and shaving months off the development schedule.

EDN *nominates EinsTimer as an Innovation in the EDA (design and implementation) category.*

INNOVATOR FINALIST Rich Perego, Rambus

Rich Perego led the design team that developed DPP (Dynamic Point-to-Point), a memory-interface technology that provides system engineers with speed and flexibility and eliminates signal-integrity issues that can arise with conventional interfaces as memory speeds increase. In six years with Rambus, Perego has earned the titles of senior principal engineer and distinguished inventor. He holds 28 either issued or pending patents.

Conventional multidrop-memory topologies allow for expansion by inserting additional memory modules but face inherent speed limits that signal-integrity issues impose. Point-to-point topologies, by their nature, provide better signal integrity but don't allow the addition of expansion modules. DPP attempts to deliver the best of both worlds through a clever design that allows a configuration with a single memory module to morph into a dual-module topology that still provides a point-to-point connection to each module.

DPP has achieved a high-profile design win in XDR (extreme-data-rate) memory, which is slated to appear in Sony's forthcoming PlayStation 3. A lone XDR-enabled module supports 12.8 to 25.6 Gbytes/sec of peak bandwidth using 32 data-signal pairs—as much as eight times the bandwidth of other approaches using half the data-bit width.

EDN *nominates DPP as an Innovation in the Digital SOC IP category.*

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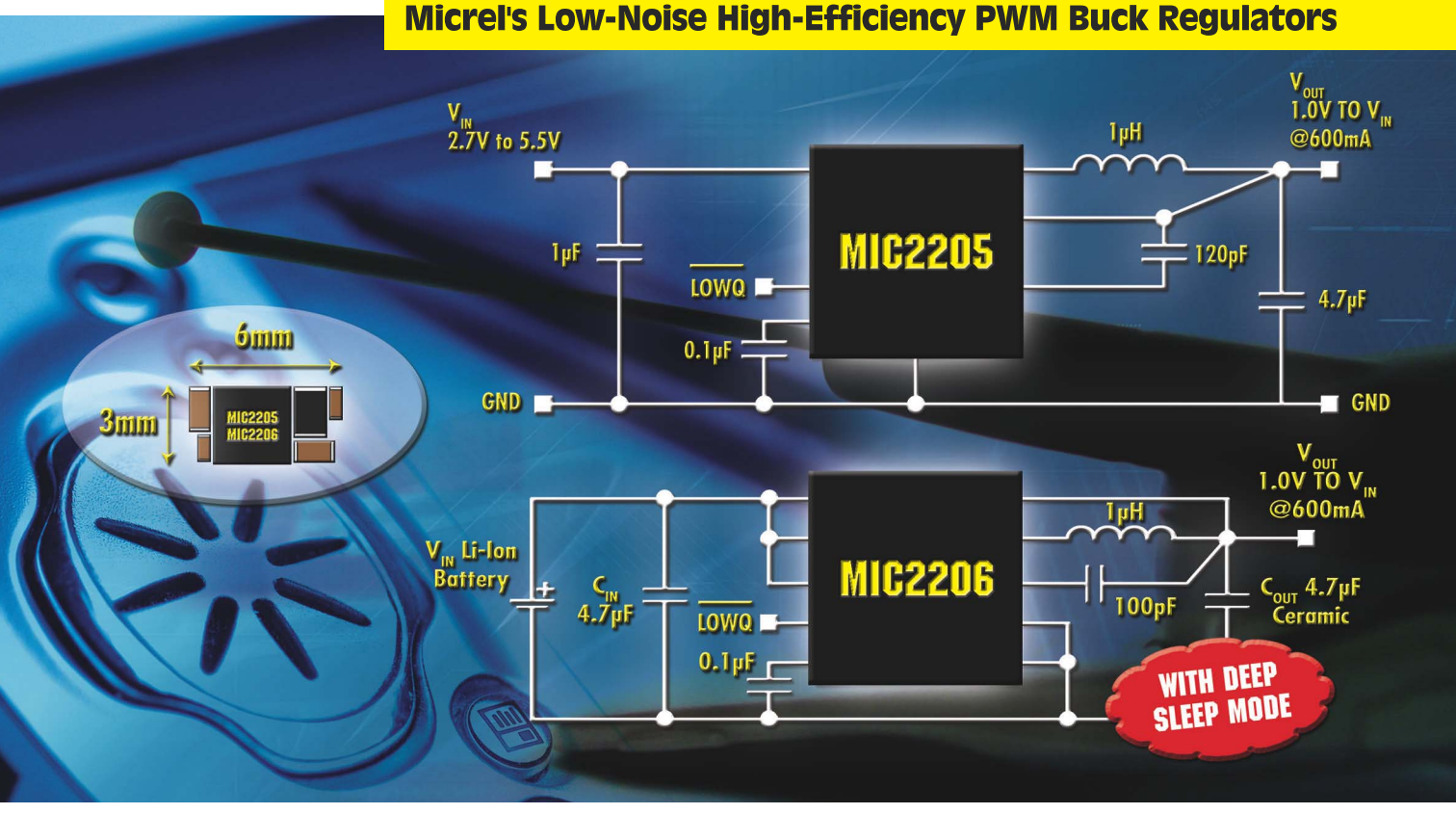
Micrel's Low-Noise High-Efficiency PWM Buck Regulators



Remember the good old days when chipset designers used LDOs to solve their portable power needs? LDOs were quiet, simple, easy to use. Then, along came lower output voltages and with them, DC-to-DC converters – highly efficient, but noisy and sensitive to placement. Now, Micrel has given designers the best of both worlds: the efficiency of a DC-to-DC converter with the low noise of a LDO.

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- MIC2205 – Adjustable output voltage option down to 1V (fixed output voltage options available)
- MIC2206 – Output Voltage Scaling (1V output in LOWQ Mode)
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EDN's 2005 Innovation Finalists

Analog ICs

Othello-G quad-band GPRS/GSM transceiver (Analog Devices)
EL7900 light-to-current converter (Intersil)
VIP50 process and products (National Semiconductor)
XC 3028 RF-to-baseband receiver (Xceive)

ASSPs and SOCs

AT78C4050 HD DVD SOC (Atmel)
DIB7000-H DVB-H receiver (DiBcom)
SPEAr customizable SOC (STMicroelectronics)
DA710 digital-audio processor (Texas Instruments)

Communication ICs

AGN300 802.11 a/b/g True MIMO chip set (Airgo Networks)
MB87M3400 WiMax SOC (Fujitsu Microelectronics)
MSM7500 CDMA chip with integrated 3-D core (Qualcomm)
OneEdge Ethernet/802.11 switch-processor family (SiNett)

Digital ICs and programmable logic

Fusion mixed-signal FPGA (Actel)
HC2xx HardCopy II (Altera)
mSerDes (Fairchild Semiconductor)

Digital SOC IP

Integrated HiMOS NVM flash (AMI Semiconductor)
SiPFlow platform-memory IP (Inapac Technology)
Dynamic Point-to-Point (DPP) technology (Rambus)

EDA (design and implementation)

X-Architecture design solution (Cadence Design Systems)
EinsTimer statistical timing (IBM Research)
Quartz DRC and Quartz LVS physical-verification software (Magma Design Automation)
Synplify Premier FPGA-physical-synthesis software (Synplicity)

EDA (verification and analysis)

PsiWinder critical path and clock-tree-timing analysis tool (Apache Design Solutions)
SLEC sequential-equivalence checker (Calypto Design Systems)
FireBolt full-chip thermal-analysis software (Gradient Design Automation)
Questa advanced functional-verification platform (Mentor Graphics)

Embedded systems

ETXexpress-PM COM Express module (Kontron America)
XPort AR embedded-processor module (Lantronix)
EPIC Express specification (Micro/sys, WinSystems, VersaLogic, Octagon Systems, Ampro Computers)

Power ICs

LM5005 integrated buck regulator (National Semiconductor)
Si8250 digital-power-supply controller (Silicon Laboratories)
STw4141 dc/dc-converter IC (STMicroelectronics)
ZL2005 digital-power-management and -conversion IC (Zilker Labs)

Power systems and modules

DPL20C PMBus-compliant POL converter (Artesyn Technologies)
iMP digital ac/dc switching power supplies (Astec Technologies)
LTM4600 high-power dc/dc micromodule (Linear Technology)
BMOD2600-48, 48V multicell Boostcap ultracapacitor module (Maxwell Technologies)

Processors

CT3600 multicore DSP (Cradle Technologies)
MPC8548E communication processors (Freescale Semiconductor)
TMS3206455 DSP (Texas Instruments)

Sensors and components

ADNS-6010 laser-based optical-mouse sensor (Avago Technologies)
MMA7260Q three-axis MEMS sensor (Freescale Semiconductor)
MLX90316EDC rotary sensor (Melexis)
MagRJ45 power-over-Ethernet connector (Tyco Electronics)

Software

Altium Designer 6.0 (Altium)
SigmaStudio (Analog Devices)
LabView 8 (National Instruments)

Test and measurement (application specific)

N4903A high-performance serial BERT with jitter-tolerance testing (Agilent Technologies)
ACE 400NB, azimuth MIMO channel emulator for WiFi (Azimuth Systems)
BERTScope CR and BERTScope CR HS clock-recovery instruments (SyntheSys Research)

Test and measurement (broad application)

WaveExpert near-real-time digital oscilloscope (LeCroy)
PXI-5922 flexible-resolution digitizer (National Instruments)
TLA7000 series logic analyzer and application software Version 5.0 (Tektronix)

BEST CONTRIBUTED ARTICLE

- **"S-parameters and digital-circuit design," by Jeff Loyer, Intel, Feb 3, 2005,** www.edn.com/article/CA498770.
- **"How to read a semiconductor data sheet," by Ron Mancini, Texas Instruments, April 14, 2005**, www.edn.com/article/CA514964.
- **"Sound advice for Class D amplifiers," by Dave Brotton, Zetex Semiconductors, April 28, 2005**, www.edn.com/article/CA526331.
- **"Filters in a nutshell: Spreadsheet promotes intuitive feel," by Dave Van Ess, Cypress MicroSystems, June 9, 2005,** www.edn.com/article/CA605510.
- **"Minimizing switching-regulator residue in linear-regulator outputs," by Jim Williams, Linear Technology, Dec 5, 2005,** www.edn.com/article/CA6288040.

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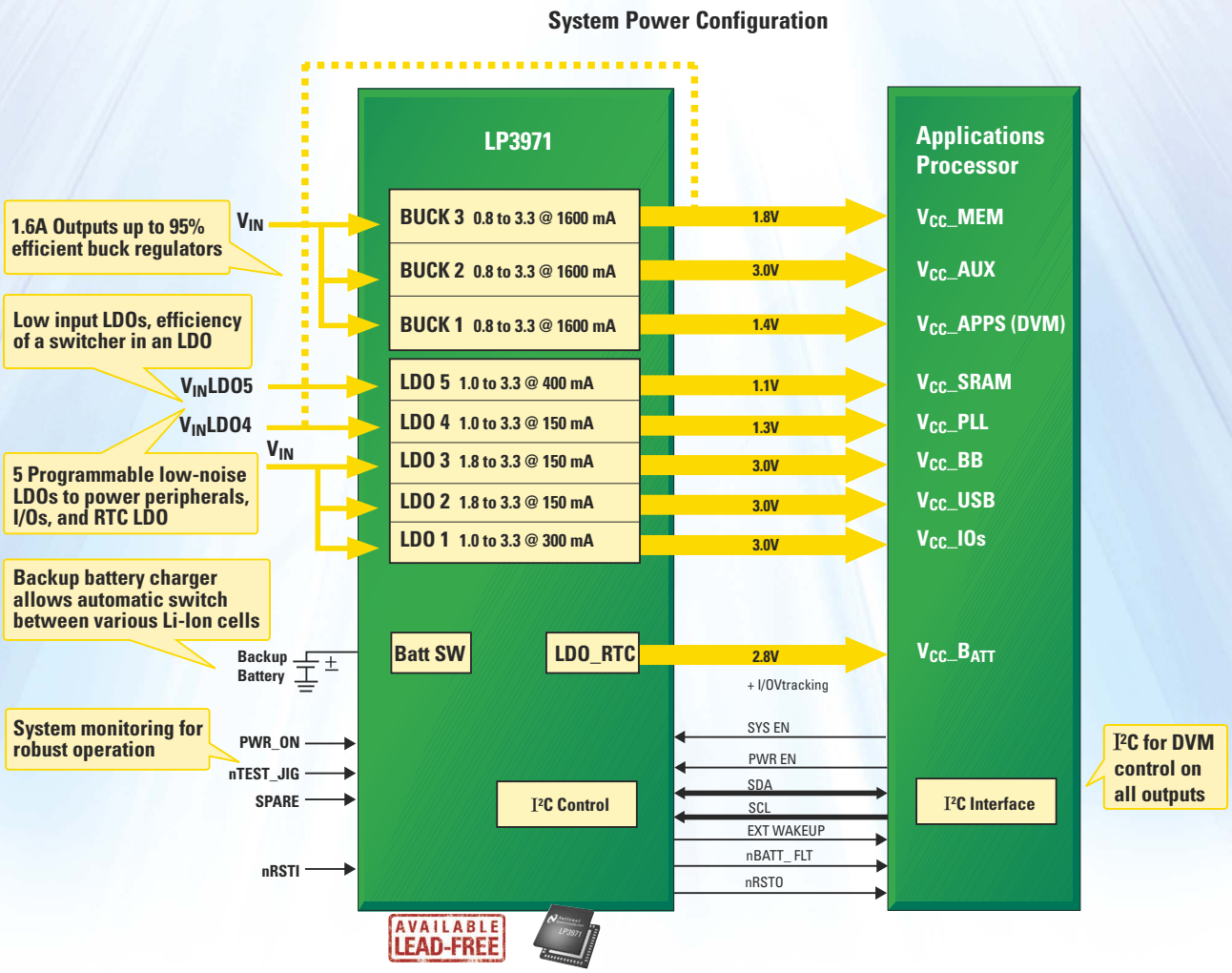

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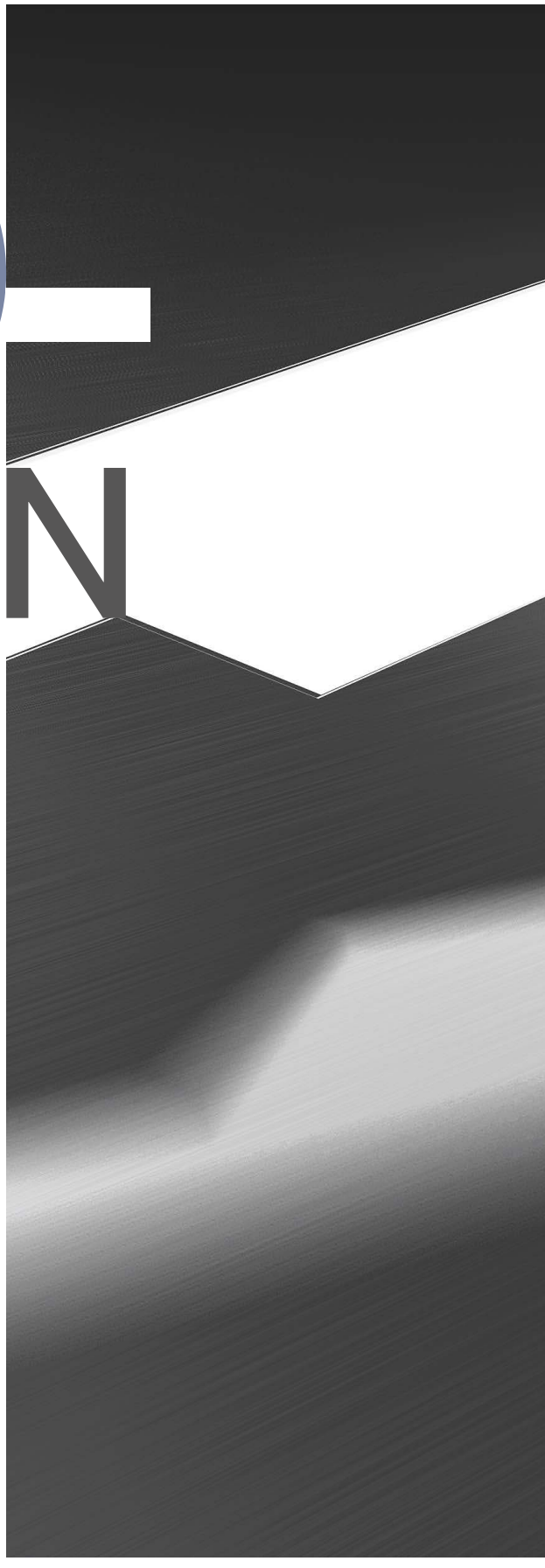
BY MICHAEL SANTARINI • SENIOR EDITOR

CO-DESIGN

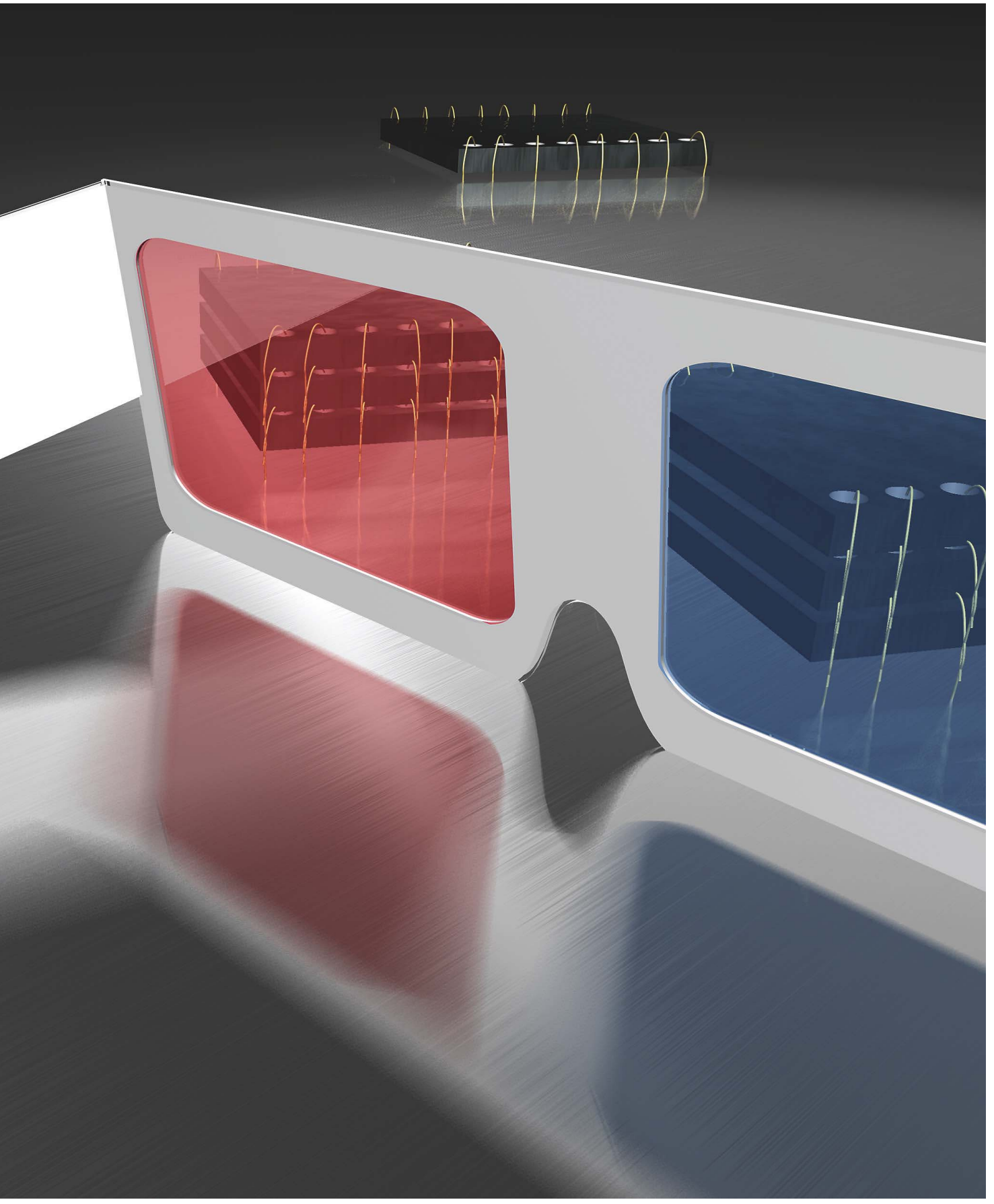
EDA VENDORS ARE HELPING IC AND PACKAGE DESIGNERS MORE EFFECTIVELY WORK TOGETHER.



Traditionally, separate groups designed ICs and packages, but cost, time-to-market issues, and ever-growing package complexity—especially as SIPs (systems in packages), multichip modules, and stacked die become more common—are now forcing IC and package designers to work together more closely. Luckily, a few EDA players, such as Cadence Design Systems, Synopsys, Magma Design Automation, Ansoft Corp, EEsof, Optimal Technology, and Rio Design Automation are now making concerted efforts to develop tools to help IC designers and package designers collaborate more effectively.

THE TRADITIONAL FLOW BREAKS DOWN

A decade ago, IC-design teams would create the IC design and, during the place-and-route phase of the process, pull up an Excel spreadsheet to outline the I/O-ball or -pin requirements and assignments. They would then throw the spreadsheet over the wall to the package-design group. Package designers would use mechanical CAD tools, such as AutoCAD or proprietary tools, to create the package based on that specification and later adjust the system as test silicon became available.



AT A GLANCE

- A decade ago, designers developed packages mainly with mechanical CAD tools.
- Early EDA-package-design tools were warmed-over pc-board-design tools.
- TSMC's reference flow 5.0 demanded that vendors offer IC-package co-design tools for 90-nm designs.
- SIPs (systems in packages) are becoming alternatives to SOCs (systems on chips) and are especially popular with companies addressing fast-moving markets.
- EDA vendors are watching SIP progress to determine whether an opportunity to develop specialized SIP-design tools exists.

Groups usually indicated to each other that changes were necessary by reworking the numbers on the spreadsheet.

The process wasn't the smoothest, but it wasn't too painful. However, as transistor counts and I/O increased, working from a spreadsheet became impractical. Additionally, many of today's designs incorporate high-speed RF and use serial interconnect instead of parallel buses, which means that designers have to deal with blistering signal speeds and thus signal-integrity, power, and thermal issues requiring more thorough circuit and EM (electromagnetic)-simulation and analysis among the IC, package, and pc board.

To better deal with these emerging issues, many companies started employing signal-integrity specialists, responsible for analyzing signals through the die, package, and board. Traditionally, companies have hired one or a few of these signal-integrity gurus to work across several design groups. These experts typically use 3-D field solvers, EM simulation, and pc-board signal-integrity tools to trace signals across the IC, package, and board.

To further sidestep some of these nasty effects, package designers adopted more advanced package materials, including moving from wire-bond to flip-chip packaging and even employing fan- or liquid-cooled packages. Of course, increasing the complexity of the package also increases its cost. Some analysts suggest that the package can have a higher per-unit cost than the die itself. Even conventional packages are growing in complexity, but that complexity jumps exponentially with designs that employ SIPs.

Despite the popular belief that a SIP is a poor man's SOC, SIPs are becoming useful in certain niches and popular with vendors addressing fast-moving markets and designers who simply don't want to deal with mixing technologies, such as analog and digital, on a single die. Flash-vendor M-Systems is a good example of a vendor that migrated from an SOC architecture to an SIP (see **sidebar** "'M' isn't for 'monolithic' at M-Systems"). But implementing an SIP or even an advanced single-die package and its extra design challenges, especially in extraction and analysis, increases the necessity for IC and package designers to collaborate more closely (see **sidebar** "A tale of two methodologies").

Jaime Metcalfe, vice president of SIP marketing in Cadence's Allegro systems division, says the old throw-the-die-over-the-wall method doesn't work any longer, even in engagements with packaging-design companies. In fact, he says, it is becoming more common for customers to demand that IC designers and ASIC houses design to specific pinout configurations, so that the design will fit into the pc board. This situation holds especially true in the mobile-handset market. "The pc board is a major cost component of a cell phone," says Metcalfe. "By getting the pins optimized, cell-phone manufacturers are able to meet performance goals and reduce layers in the pc board. That [approach] cuts cost."

EVOLUTION OF TOOLS

EDA vendors have attacked IC and package co-design from two directions: upstream with IC-optimization tools and downstream with pc-board-systems tools. The industry's first step toward bringing together IC design and package design with an IC-centric approach occurred when vendors started integrating I/O-pinout-assignment software into IC-physical-implementation tools. Doing so, says Keith Felton, SIP-product-marketing-group director for the Allegro group at Cadence, eliminated the manual task of creating assignments in a spreadsheet.

"It is especially important with designs that have high-speed signals like

"M" ISN'T FOR "MONOLITHIC" AT M-SYSTEMS

When M-Systems many years ago introduced its MDOC (monolithic-disk-on-chip) hybrid boot-from-NAND device, a single die integrated the NAND core and NAND controller and software functions in an SOC (system on chip). Ariel Mashkovitz, vice president of the M-Systems Mobile Division, says that M-Systems quickly found out that it is impractical to develop a new SOC for every NAND and NAND density, especially as NAND suppliers rapidly increase density grades in what has become a hot market.

Therefore, M-Systems went to an SIP (system-in-package) model, which maintains the controller and related software on one IC and the NAND on another. The company can adjust the software in the controller to pair it up with a variety of NAND devices from disparate vendors and densities in a single package. This ability means that M-Systems can quickly swap out a lower bit NAND if a higher density NAND emerges during a customer's product development. Today, the SIP model is such a force at M-Systems that the company renamed the product as "mobile," rather than "monolithic," disk on chip.

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SERDES [serializers/deserializers]," says Felton. "You don't want to end up putting so much skew in the die that it is impossible to rectify it in the package."

IC-floorplanning tools from Cadence, Synopsys, and Magma have for a few years had I/O-pinout-assignment features, but Felton says that traditional floorplanning tools don't go far enough, because they have only a rudimentary view of the package.

EDA vendors have also attacked the problem from the pc-board-fabric side. In the mid-1990s, Cadence created a variant of its pc-board tools for package designers. That tool, Advance Package Designer and, shortly after, tools from Avanti (which Synopsys has since acquired) brought commercial electrical design and analysis to package designers. Those tools had schematic entry and layout and autorouting for packages but lacked a useful link to IC design and even a link to simulation and analysis. Cadence and a growing field of players over the last three years have made even more significant strides in IC and package-co-design technology.

THE NEW GENERATION

An-Yu Kuo, chief technology officer at Optimal Corp, says that EDA-industry efforts to develop IC- and package-co-design tools sped up in 2004, when TSMC (Taiwan Semiconductor Manufacturing Co) issued its reference flow 5.0, which highlighted the need for an IC- and package-co-design flow (**Reference 1**). "Today, there are still no cohesive co-design tools, and, in the past, IC and package design were isolated islands," says Kuo. "Three years ago, TSMC recognized the importance of IC and package co-design for nanometer flows, and the industry has since responded. The EDA industry has made great progress, but we're not all the way there yet."

Cadence, largely because it already had many of the point tools in the market, was the first to piece together a flow (**Figure 1**), and most package-design point-tool vendors tailor tools to fit the Cadence package-design flow. A year ago, Cadence enhanced its co-design offerings by releasing package- and pc-board-co-design capabilities with Allegro Package SI (signal-integrity) 620. That tool adds Optimal Corp's 3-D field-solver engine to the Allegro Package SI simulator. The 620 tool reads and writes package designs produced and designed by Allegro Package Designer as well as pc-board designs created with the Allegro pc-board-layout tool. It allows users to make trade-offs between their board layout and electrical effects.

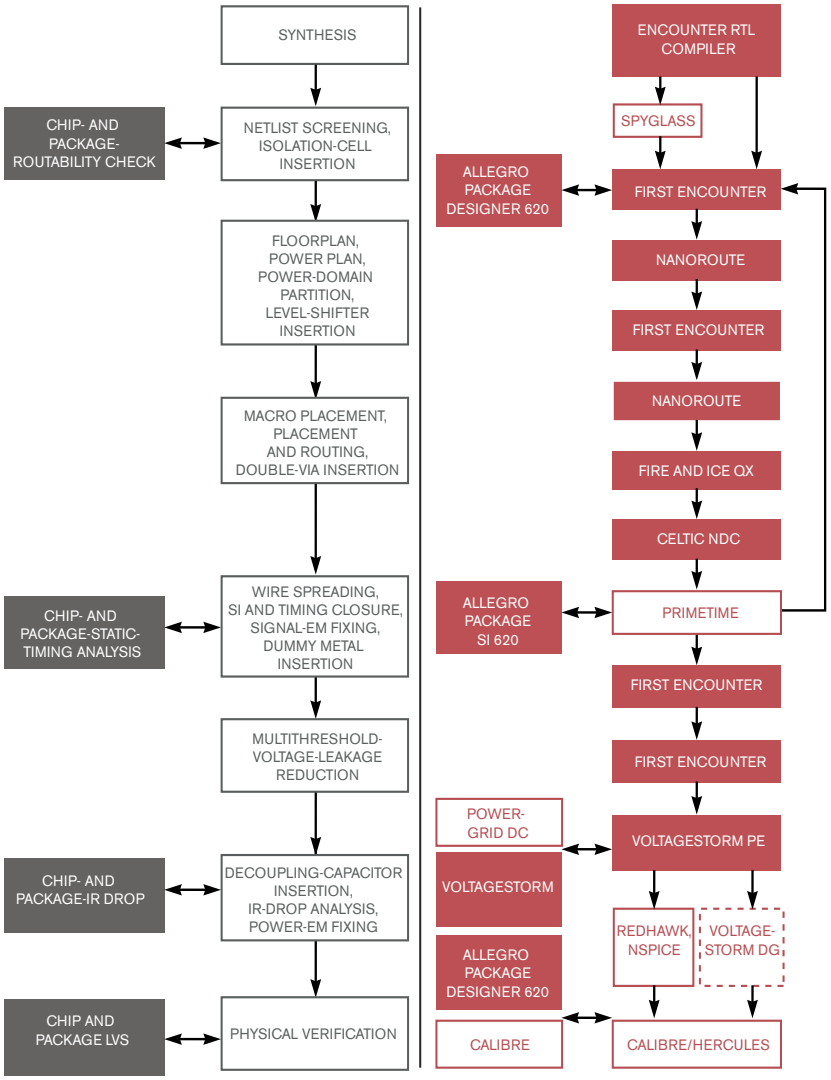

Figure 1 Cadence—an early innovator in package design, as well as in pc-board- and IC-design tools—has been able to respond to TSMC's request for an IC- and package-co-design-tool flow.

"We wanted to help users analyze the electrical pathway from the die all the way through to the pc board and optimize to the final mask the quality level of the package substrate as well as the pc-board substrate," says Felton.

Synopsys, too, has stepped up its efforts. The company gained the Xynetix package-design tool in its 2001 acquisition of Avanti, but, in September 2005, Synopsys took a step toward further automating the flow with JupiterIO. The tool is a concurrent die- and package-I/O-planning tool that includes I/O and bump placement, RDL (redistribution-layer) routing, and some package-route planning, as well. It accesses IC data through the Milkyway database and packaging data through standard interfaces.

The IC- and package-co-design market even has a start-up. By press time, Rio

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ADS5444	13 Bits	250 MSPS	68.6 dBFS at 230 MHz IF	78 dBc at 230 MHz IF
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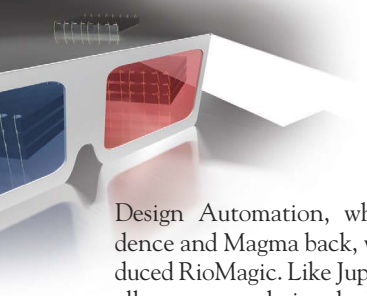

Design Automation, which both Cadence and Magma back, will have introduced RioMagic. Like JupiterIO, the tool allows users to design the IC and package concurrently instead of sequentially (**Figure 2**). Kaushik Sheth, Rio's chief executive officer, says that the flow allows IC designers to make "packaging-aware" adjustments to their IC designs, and if changes in the board or packaging are required, the IC design can instantly reflect those changes. In the RioMagic flow, users build and work from a single golden I/O data model at the IC-floorplanning stage that the rest of the flow accesses through Si2's OpenAccess.

Joel McGrath, vice president of marketing at Rio, says that RioMagic analyzes

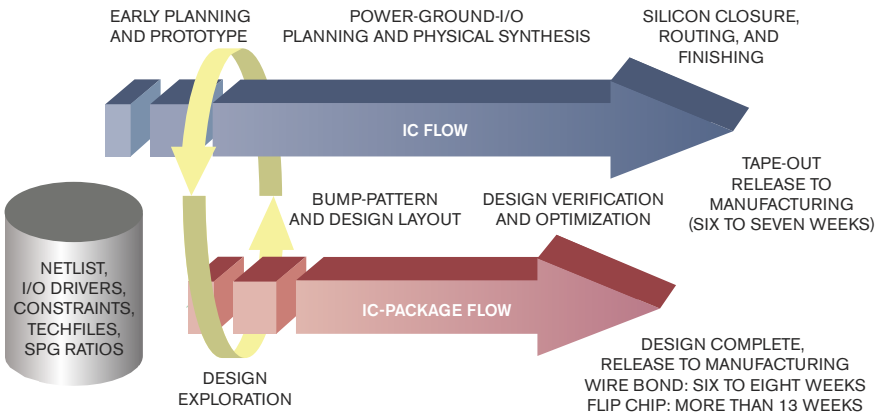

Figure 2 With Rio Design Automation's RioMagic, designers work from the same model and design ICs and packages concurrently, instead of sequentially.

A TALE OF TWO METHODOLOGIES

IC- and package-design challenges commonly confront today's ASIC vendors. LSI Logic and NEC run into similar problems regarding co-design but attack them using slightly different methods and tools.

LSI Logic uses an integrated team to ensure that designers take packaging concerns into account at the beginning of the process. Yogi Ranade, marketing manager at LSI Logic, says that a design team at LSI typically includes ASIC designers, a die and package signal-integrity specialist, a package designer/layout specialist, and a systems/methodology engineer. "They all talk upfront and do quick what-if scenarios," says Ranade. "Since they talk different languages, they use different tools."

Ranade says that, at LSI, a signal-integrity engineer typically uses Ansoft's Turbo Package Analyzer or an Optimal Technology 3-D field solver. The package designer uses an APD (application-parameter-descriptor) tool from Cadence, and IC-design engineers use the usual ASIC tools.

Ranade says that, although current-generation commercial tools support standard formats and thus teams can transfer files back and forth, the cross-discipline design and analysis flow needs improvement.

"What would be neat is if in the packaging environment you could do a quick-turn, what-if signal-integrity analysis that would tell you that nicking down a trace would cause a discontinuity," says Ranade. "It would allow you to create better signal-integrity limits for the IC design. That what-if analysis doesn't happen as quickly as we'd like to see it."

Ranade says that anything that could help system-level engineers share their pains with IC and package engineers would help further improve the methodology. "Today, on the silicon side, we have redistribution layers on top of the silicon where we route out to the wire-bond pads," says Ranade. "We are doing a lumped analysis in this area, but we think that EDA tools could help us more effectively route to wire-bond pads."

Han Park, a senior engineering manager at NEC Electronics America, says that NEC has a specialized packaging-design group that works closely with IC designers. Because the EDA industry has been slow to develop a tool flow, the group has developed its own design software and methodology.

"A couple of years ago, we found that you just can't design the package by itself any longer," says Park. "You really have to consider the silicon and the package together."

Park notes that, with an early understanding of package problems, IC designers can place functions on their layout so problems don't occur during packaging. And if packaging designers know about silicon problems early, they can add functions or shielding, such as decoupling capacitors, to problem areas on the package.

The NEC tool incorporates RLC extraction, as well as signal- and power-integrity analysis. It currently supports flip-chip packaging, but company tool architects are developing a version for wire-bond design for deployment early this year.

Park doesn't believe NEC will offer the tool commercially, but he says that the company is constantly evaluating commercial offerings and would move to one if the EDA industry were to offer a flow superior to NEC's.

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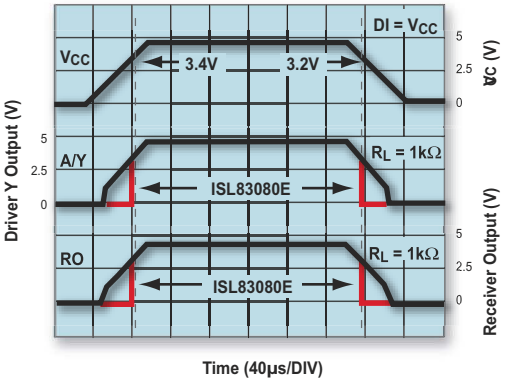

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ISL83082E	1 / 1	256	Half	Yes	Yes	0.115	Yes	Yes	560 / 530	0.07	4.5 to 5.5	8 Ld MSOP 8 Ld SOIC
ISL83083E	1 / 1	256	Full	Yes	Yes	0.5	Yes	Yes	530 / 530	0.07	4.5 to 5.5	14 Ld SOIC
ISL83085E	1 / 1	256	Half	Yes	Yes	0.5	Yes	Yes	560 / 530	0.07	4.5 to 5.5	8 Ld MSOP 8 Ld SOIC
ISL83086E	1 / 1	256	Full	Yes	No	10	No	Yes	530 / 530	0.07	4.5 to 5.5	14 Ld SOIC
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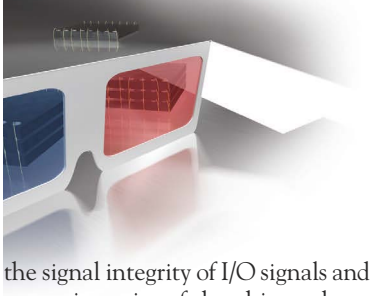

the signal integrity of I/O signals and the power integrity of the chip package. To do so, RioMagic builds electrical models that capture on-chip as well as package parasitics. To build the on-chip part of the model, RioMagic precharacterizes on-chip interconnects and stores them in look-up tables.

For the package part of the electrical model, RioMagic extracts the RLC and K and builds a detailed PEEC (partial-equivalent-electrical-circuit) model of the package. This PEEC model captures the entire package without incurring the cost of running a field solver. The tool also generates a simulation deck with primary drivers, drivers for coupled nets, a coupled-net parasitic network, and a pc-board-loading termination for each net. The tool analyzes this network and then calculates the response for the primary net switching and any coupling effects from adjacent nets.

AN SIP OFTEN INCORPORATES A MIXTURE OF ANALOG AND DIGITAL ICs, USUALLY SIDE BY SIDE RATHER THAN STACKED, TO ENSURE SHIELDING.

RioMagic includes a synthesis engine that uses this model to help users assign I/O and immediately see whether it has an impact on the IC floorplan. When users move hard cores, which have fixed I/O, in their floorplan, RioMagic automatically resynthesizes the rest of the I/O conforming to the model.

RioMagic works from standard formats. The tool uses DEF (design-exchange format) for chip netlist data, IP (intellectual-property) libraries for I/O, standard-cell and hard macros in LEF (layout-exchange format), and I/O-driver models in IBIS (I/O-buffer-information specification).

More advanced designs, especially those employing SIPs as well as mixed analog and digital or high-speed RF ICs, require more detailed extraction, EM analysis, and thermal analysis and simulation. Some research is even looking at incorporating antennas in SIPs. Luckily, many of the tried and true vendors, such as Ansoft, EEsof, Cadence, Synopsys, Flomerics, and Optimal, offer tools for leading-edge applications.

An SIP, for example, often incorporates a mixture of analog and digital ICs, usually side by side rather than stacked, to ensure shielding. In a two-IC SIP, designers need to perform parasitic extraction and signal- and power-integrity analysis individually on both device die and packages. Designers then have to analyze the SIP as a single unit in the context of the entire system.

The analysis can become even more complex if the die are stacked in wire bond or if the designs incorporate RF blocks with high-speed signals, which are susceptible to interference from the digital blocks. The amount of data extracted can be unwieldy, often forcing users to employ model-based techniques.

Both EEsof and Ansoft offer 2-D planar and 3-D EM simulators. Although RF tools typically evolve at a snail's pace, Ansoft recently introduced the Nexxim circuit simulator, which noted Massachusetts Institute of Technology professor Jacob White developed, to complement the company's flagship HFSS (high-frequency structured simulator). Nexxim uses the same circuit netlist and library models for transient and harmonic-balance analyses. Larry Williams, director of marketing at Ansoft, says that

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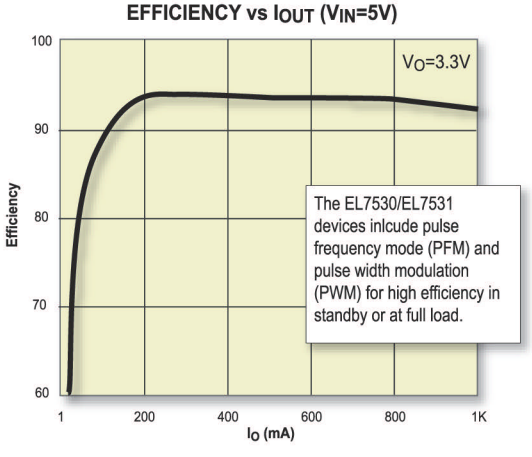

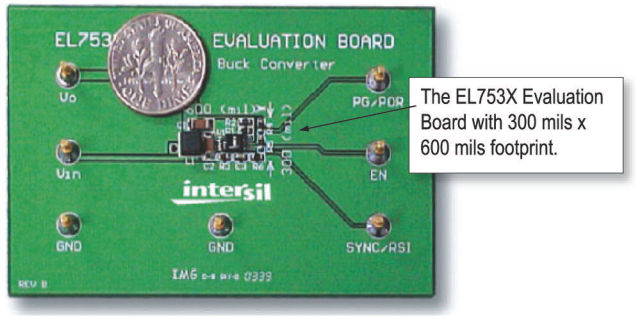

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the tool offers increased runtimes, making it practical for use in IC, package, and pc-board design with a mixture of models. With this approach, designers need not reconcile differences between running analyses on different simulators, each running from separate netlists and device models.

"There are the challenges we've always had for creating a model for electromagnetic, with extracting it so it is accessible to the design engineer," says Williams. "But, once you have that model, what do you do with it in your circuit simulator? If you use a traditional parasitic extractor on chip, for example, you rapidly overwhelm your circuit simulator. Most folks say go to a fast Spice simulator, but often you are making oversimplifications for the active devices. What is needed is a better circuit simulator. That's why [Ansoft] developed Nexxim."

Ansoft also offers the Turbo Package Analyzer, a package-modeling tool that employs boundary-element methods for high-pin-count BGA packaging.

Agilent's EEsof group also offers Momentum, an advanced 3-D planar EM tool. The company recently released a 64-bit version of the tool to deal with the capacity issues that field solvers present.

Thanks largely to TSMC's putting IC and package co-design on its reference flow for 90-nm design, the EDA industry is starting to ramp up its efforts in IC and package co-design. Although EDA companies are stepping up their game, they are far from conquering all the challenges in this area. Most vendors admit that, if SIP continues its growth, a greater need will emerge for IC integration and perhaps opportunities for EDA vendors to develop a subflow for SIP designs. It remains to be seen, however, which design group is responsible for the SIP: the IC-design group, the package-design group, or the system-design group. Perhaps SIP design will become so complex that it will require a new, specialized designer or design team. We'll see. EDN

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2 www.fractus.com/aip.htm.

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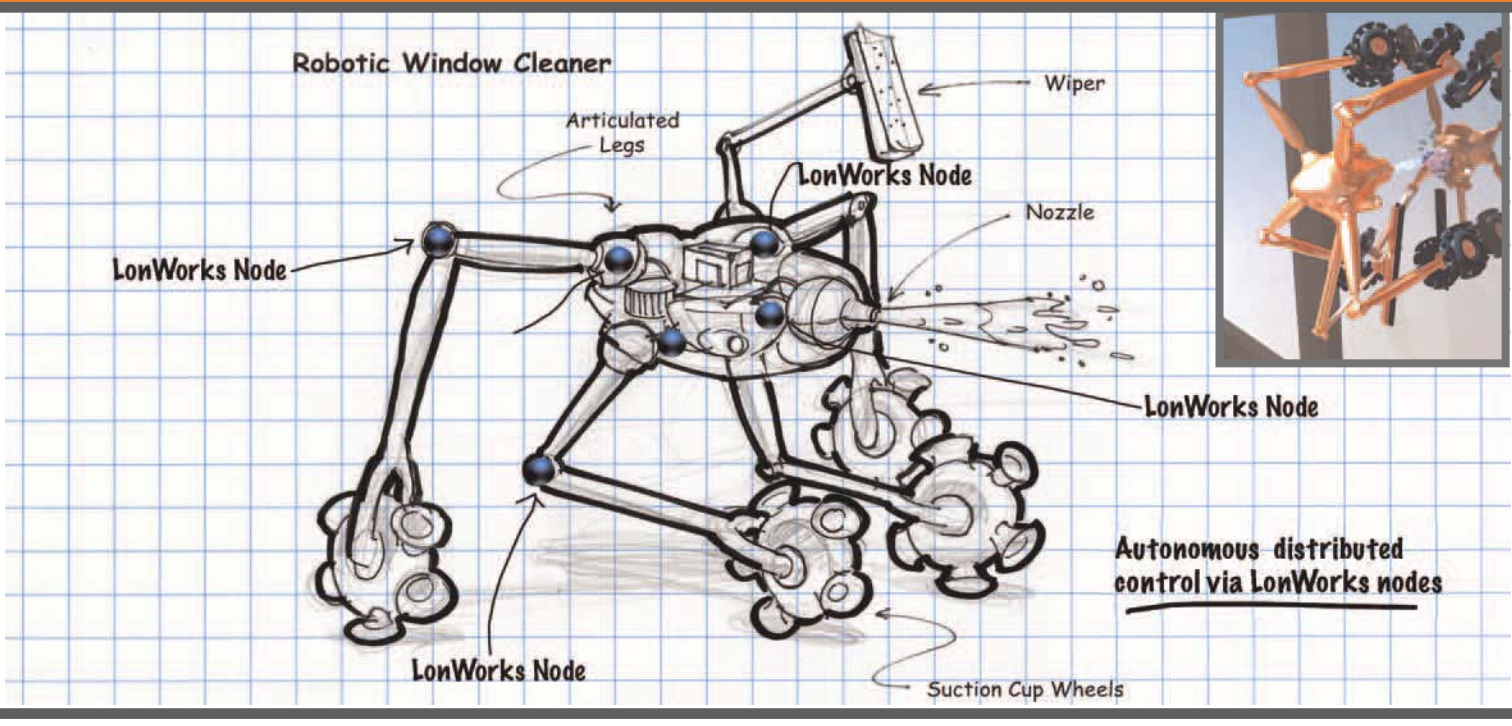

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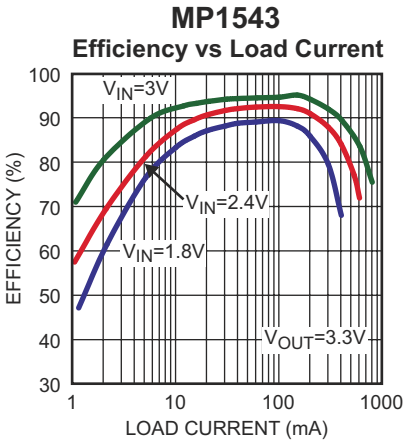

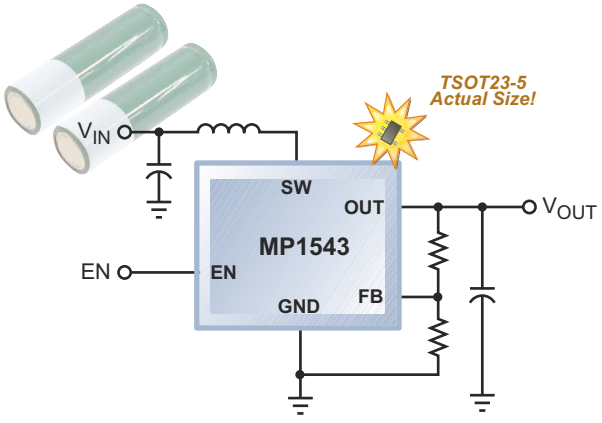

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MP1542	2.5 - 22	22	0.7/1.3MHz	MSOP8
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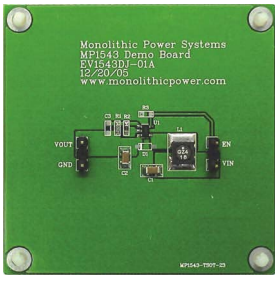

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FRIEND OR FOE:

Battery-authentication ICs separate the good guys from the bad

ALL BATTERY PACKS ARE NOT CREATED EQUAL: UNAUTHORIZED AFTER-MARKET PACKS MAY CONTAIN CELLS THAT CAN SELF-DESTRUCT WHEN YOU CHARGE THEM AT THE HIGHER VOLTAGES THAT NEW LITHIUM-ION TECHNOLOGIES DEMAND. BATTERY-AUTHENTICATION ICs USE ADVANCED SECURITY METHODS TO WEED OUT COUNTERFEITS.

Battery packs for consumer applications, such as cell phones and laptops, continue to move further away from the one-size-fits-all category. The responsibility for ensuring that only compatible packs plug into recharging systems again belongs to the system designer to authenticate a battery pack before charging it. To decide which authentication scheme is right for your design, you need to weigh the cost, size, and security level that chip vendors' authentication approaches are now offering.

Battery-pack authentication is necessary because the lithium-ion cells that are the building blocks of all such packs are changing, and, although they still may have the same physical dimension, their input charging voltage and required charging rates are changing and fragmenting across markets (**Reference 1**). If the cells charge at the wrong voltage or too quickly, they may explode. Vendors can ship their products with the proper battery pack, only to find that customers go the after-market route to replace or back up battery packs because after-market packs are easy to find and usually cheaper. Counterfeit battery packs pose a threat to user safety (**Reference 2**).

In 2004, cell-phone manufacturers Kyocera and LG both had to recall branded, counterfeit battery packs that lacked the necessary overcharging circuits to prevent overheating and explosions. To combat such problems, one cell-phone manufacturer, Nokia, places holograms on its approved battery packs. Customers can check the code on the hologram online to verify whether a part is genuine. However, this approach assumes that the customer shares the manufacturer's concern about the battery pack's quality and authenticity and can evaluate the authenticity of the hologram label. A more active approach to verifying packs is to build authentication into the charging system (see **sidebar** "A primer on security cracking").

The lowest level of authentication is to verify that the battery works basically as a user expects. To perform such authentication, place a resistor into the pack and measure the voltage drop. The next level relies on reading a code in the pack that contains parameters such as battery ID, manufacturing date, and cell voltage. These parameters are easy to read and duplicate, however. The highest level of security uses a challenge-response procedure between the system host and a cryptographic-authentication IC in the battery pack (**Figure 1**). The host system can be an external, separate battery-pack charger, but, for cell phones and laptops, the battery pack usually charges while it's in the device rather than in an external charger. The authentication IC within the battery pack answers the host query

AT A GLANCE

- After-market battery packs may be unable to handle the higher charging voltages that new lithium-ion technologies require, potentially leading to unsafe, explosive conditions.
- Host systems need to authenticate battery packs before recharging.
- Authentication ICs handle the complexity of using security algorithms to validate packs.

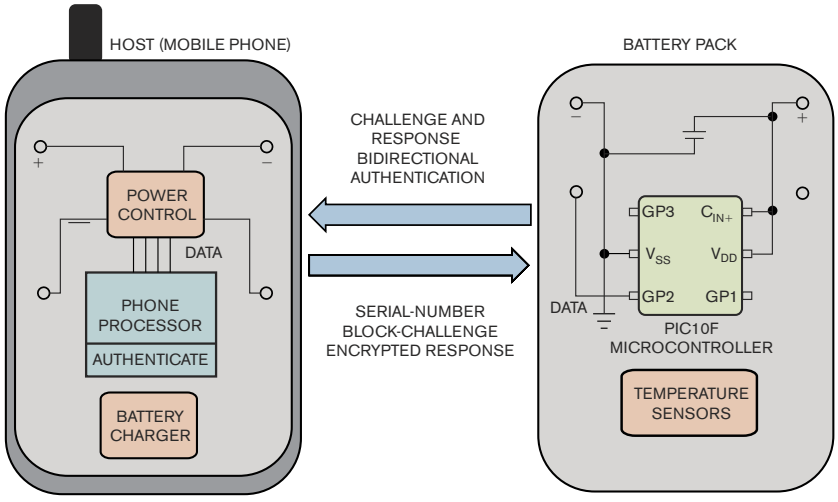

Figure 1 The host system issues a challenge to the battery pack and waits for the proper response before beginning charging to ensure that the pack is authentic (courtesy Microchip).

with a response that its security algorithm and a secret key code in the device determine.

Authentication ICs' security level depends on the complexity of their encoding algorithms. The three popular techniques that authentication ICs use are CRC (cyclic redundancy check), SHA-1 (Secure Hash Algorithm-1), and proprietary vendor algorithms (**Table 1**).

HASHING OR ENCRYPTION

Hashing algorithms calculate a signature for the system inputs and are not, strictly speaking, encryption algorithms, although people commonly refer to them as such. Encryption algorithms are two-way, allowing unlimited encoding and decoding of data streams. Hashing functions are one-way: You can't regain the input data from the signature. The NIST (National Institute of Standards and Technology) created the SHA-1 (pronounced "Shaw-one") hashing algorithm, the most popular security algorithm. It powers the NIST's digital-signature standard (**references 3** and **4**).

New ICs are offering this algorithm, measuring how seriously companies are taking battery authentication. Previously, they would have considered this feature as overkill for this application. For example, Maxim has introduced the DS2704, a SHA-1 based device, as an upgrade from the DS2502, which provides ID information only with no encryption. The DS2704 is backward-compatible with the 2502 instruction set and has an additional page of EEPROM for storing battery-condition information, such as amount of charge.

SHA-1's high security level comes at a cost: The die for such a chip must be larger because of the more complex algorithm. Jon Qian, senior member of the technical staff at Texas Instruments, which makes the CRC-based bq26150 IC, defends the CRC as a cost-effective security measure: "SHA-1 is well-known; banks use it for financial transactions, but this level of complexity requires a bigger die and more internal memory. CRC-based authentication is still difficult to break but still gives a decent die-size implementation." He concedes that high-security requirements warrant SHA-1. For example, TI plans to introduce the SHA-1-based bq26100 chip in the second quarter.

Arman Naghavi, vice president of Intersil's Handheld Power group, says that determining the amount of security you need requires balancing the life of a consumer product and the cost of the security feature. You can think of the robustness of a security algorithm in the years of computer processing it takes to break it. Intersil's ISL9206 uses the company's proprietary Flexihash+ security algorithm; Naghavi claims that it would take three Pentium 4 processors 10 years to break the code. Consumer products

A PRIMER ON SECURITY CRACKING

Gene Armstrong, managing director of thermal and battery management for Maxim, lists several ways to attack a security system for a battery pack: "One attack method is to use brute-force computing: You issue a challenge, review the response, and emulate that function on a very fast computer, looking for the secret key that generated that challenge-response pair.

The problem with brute force is that it takes 280 years to find a 64-bit secret. A 3-GHz processor can execute a SHA-1 test in about 220 nsec. To check all combinations would require 3.9^{12} sec, or about 125,000 years. Even when 10,000 engines are running in parallel at 3 GHz, this method doesn't guarantee a match for 12.5 years."

A second technique, side-channel attack, looks for a manufacturing-test mode to exploit. Armstrong points out that Maxim's DS2704 has no test modes that read the secret: For test, Maxim looks at an AND of all the bits and an OR, to ensure that that portion of the IC is working.

A third type of attack would be a physical one. Maxim bases its parts on a three-metal process, with a final metallized-silicon layer, making it difficult to read even with an electron-beam microscope.

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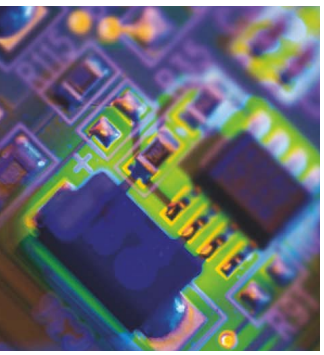

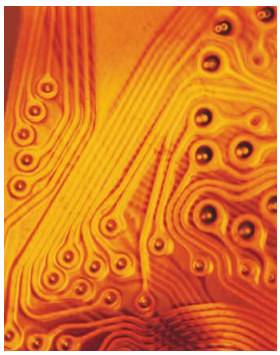

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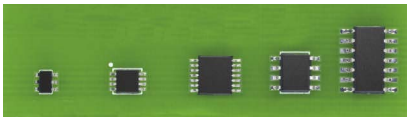
with a typical lifetime of a few years don't warrant such an effort.

SECURITY ISN'T FREE

Battery packs for consumer devices are cost-sensitive. Ken Dietz, senior applications engineer in Microchip's Security, Microcontroller, and Technology Development Division, suggests that, although battery-pack manufacturers are moving to higher security levels for battery packs, both the size and the price of the circuit still constrain them. "Battery-pack manufacturers ask us: What is the smallest device they can use, what algorithm they can fit onto that device, and how much will it cost to implement the design?" he says. Microchip offers its proprietary KeeLoq algorithm, which the automotive industry has for 10 years used for key fobs. A true encryption scheme, rather than a hashing algorithm, KeeLoq can fit into just 47 code words, allowing the algorithm to fit into Microchip's PIC 10F, which the company claims is the world's smallest microcontroller. In a six-pin SOT-23 package, it costs about 49 cents (volume quantities).

All authentication-IC vendors emphasize that poor security of a company's internal codes can stop the strongest security algorithm in the world. One of Microchip's customers keeps its secret key in an 8×8-ft vault with 3-ft-thick walls, and only two people in the company have vault keys. Gene Armstrong, managing director of thermal and battery management for Maxim, agrees that SHA-1 security depends on keeping the 64-bit key code secure: If someone within the company can steal the key, then no attempts to crack the algorithm are necessary. He explains how the DS2704 security fits into the supply chain: The company ships the part with a programmed, 64-bit key that is not the ultimate secret key. The battery-pack manufacturer assembles the IC into the pack and, as part of the assembly process, issues a challenge to the part and receives a response. The next step in the assembly process is that the process issues a command, "Compute next secret," which becomes the final key the company stores in the pack. "You can implement your supply chain so that no one source has the secret," he says. EDN



Despite being a general-purpose microcontroller, the PIC10F's size and pin count make it a candidate for handling encryption algorithms that can fit into a small block of code. Pin counts range from six (left) to 14 (right).

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For a releated article, see "Quantum cryptography: when your link has to be realy, really secure" at www.edn.com/article/CA6290450.

For more on this topic, see "Rolling-code generator uses flash microcontroller" at www.edn.com/article/CA82741.

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TABLE 1 ICs FOR BATTERY AUTHENTICATION

Vendor	Part name	Part no.	Key length	Security algorithm	No. of communication lines	Package supported	Price	Comments
Intersil	Secure authentication IC with Flexihash+	ISL9206	64	Proprietary (Flexihash+)	One	SOT23-5	$1.15 (1000)	
Maxim	1-kbit ROM	DS2502	NA	NA	One	ThinSOT	Less than 50 cents (1000)	12-byte EPROM
	SHA-1 battery-pack-authentication IC	DS2703	64	SHA-1	Three	2×3-mm TDFN	Less than 50 cents (1000)	
	1280-bit EEPROM with SHA-1 authentication	DS2704	64	SHA-1	One	3×3-mm TDFN	Less than 50 cents (1000)	160-byte EEPROM
Microchip	PIC10F microcontrollers	PIC10F	64 (KeeLoq), 128 (XTEA)	Virtually any algorithm, such as proprietary KeeLoq and open-source XTEA, is software-implementable	One or two	Six-pin SOT-23	49 cents (1000)	
Texas Instruments	Battery-pack-security and -authentication IC	bq26150	128	CRC	One	SC-70	$1.30 (1000)	96-bit ID plus 16-bit encrypted polynomial and 16-bit encrypted seed; total of 128 bits
	Battery-pack-security and -authentication IC	bq26100	128	SHA-1	Two	SC-70	Less than $2 (1000)	Introduction in the second quarter of 2006; price is approximate

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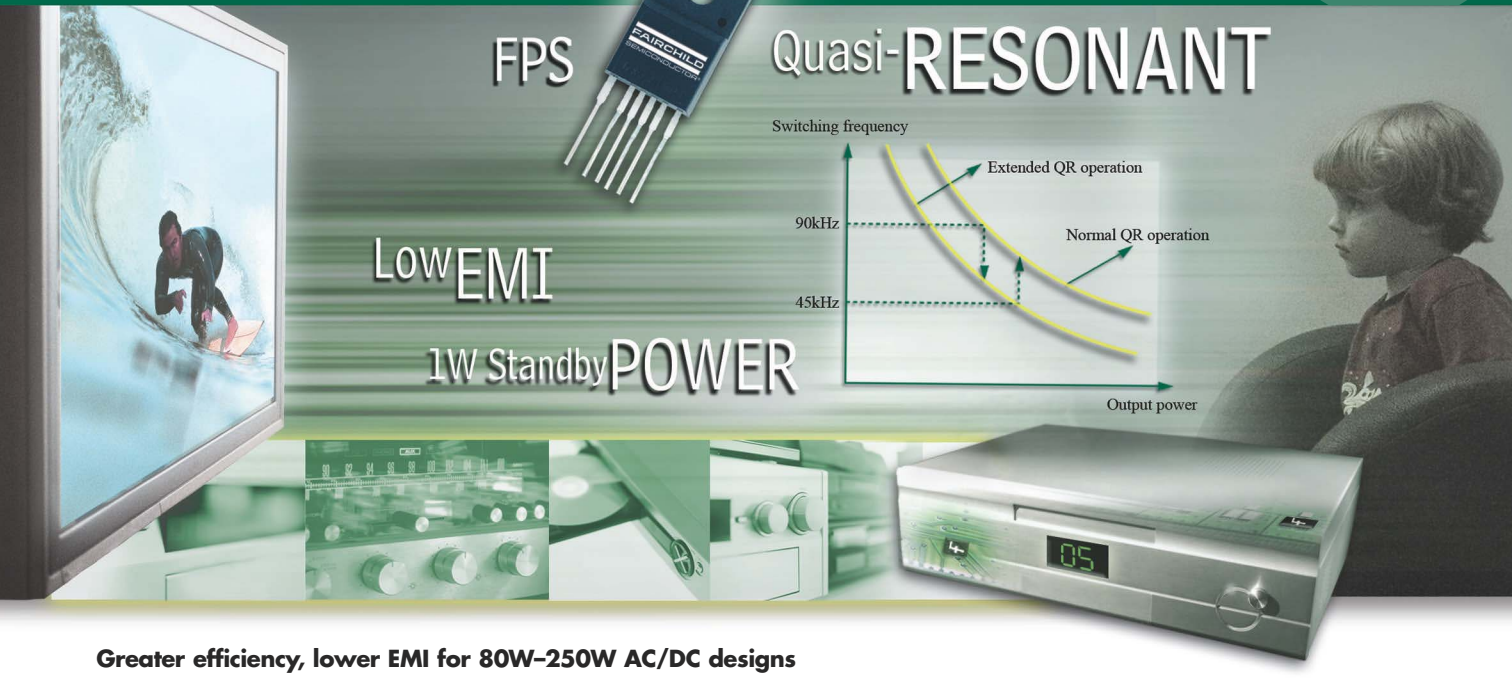

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FSCQ0765RT	85	5	1.6
FSCQ0965RT	110	6	1.2
FSCQ1265RT	140	7	0.9
FSCQ1465RT	160	8	0.8
FSCQ1565RT	170	8	0.7
FSCQ1565RP	210	11.5	0.7

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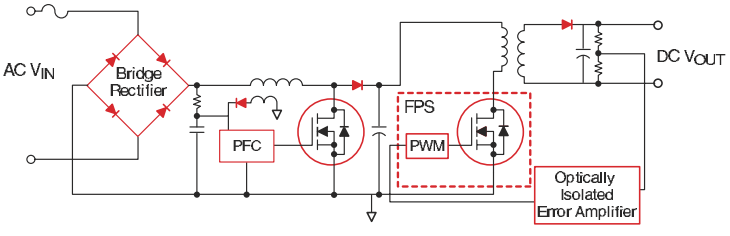

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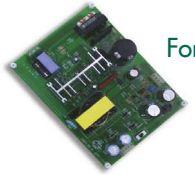

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Dual threshold voltages and power-gating design flows offer good results

DUAL THRESHOLD VOLTAGES AND POWER-GATING DESIGN FLOWS MANAGE BOTH LEAKAGE POWER AND PERFORMANCE WITH LITTLE EFFORT.

Design-optimization methodologies and flows that use gates with two threshold voltages (V_{TH}) can achieve excellent results for both power and timing with a high degree of automation. This dual-V_{TH} approach has become crucial for VDSM (very-deep-submicron) chips, in which reduced V_{TH} not only improves performance, but also increases static (leakage) power.

In fact, leakage power increases exponentially with the technology scaling and reaches 50% of chip power at 65 nm. This dramatic increase in leakage power is unacceptable for most designs, whether or not they run from battery power. As a result, most designs can benefit from design-optimization flows that balance the trade-offs between performance and leakage power.

There are three popular flows for optimizing performance and leakage power based on design requirements. These flows target minimum leakage, best performance, and optimum chip area and tool runtime for a design in power-on mode. Because the design still consumes leakage power in standby mode, the flows also include methods for minimizing standby leakage power.

THREE FLOWS FOR MANAGING LEAKAGE POWER

Dual-V_{TH} methodologies rely on the use of two cell libraries—one with low-V_{TH} cells that have smaller propagation delay and higher leakage power, and the other with higher V_{TH} cells that have larger delay and lower leakage. Optimizing a design with the low-V_{TH} cells in critical timing paths and high-V_{TH} cells in noncritical paths can maximize speed and minimize leakage power.

The quality of this optimization depends significantly on the identification of true timing-critical paths and accurate calculation of the two libraries' timing impact on a path. To achieve the necessary timing accuracy, path-delay calculations need to include interconnect delays based on cell placement and net-routing information. Thus, physical synthesis is highly recommended for the second-pass mixed-V_{TH} design optimization in the following three flows:

- The min-cut flow achieves the lowest leakage power of the three flows but has higher cell count and dynamic power as well as lower performance.
- The max-cut flow results in the highest performance and lowest cell count and dynamic power but has the highest leakage power of the three flows.
- The max-cut II flow provides a compromise of the first two approaches with a good balance between leakage power and chip area. This flow also minimizes tool runtime and capacity issues.

The first flow uses an iterative min-cut algorithm, in which all cells in a combinational circuit are initially assigned a high threshold voltage. Due to the performance degradation of the high-V_{TH} transistors, the design usually violates delay constraints. But the initial design has the lowest leakage power. Next, the algorithm identifies a minimum subset of edges, in which changing threshold voltages to low improves the performance and meets the delay constraints. A min-cut graph algorithm based on minimum-weight cut identifies these edges.

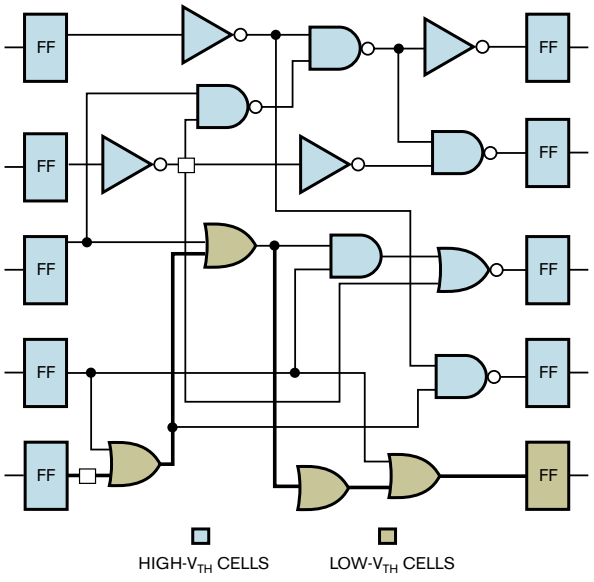

Figure 1 In this example of the min-cut approach to reducing leakage-power consumption, the synthesis tool has swapped logic gates in the critical paths to low-V_{TH} gates to meet timing constraints.

This cut corresponds to the smallest power increase as a result of changing to low V_{TH}. **Figure 1** shows an example of the dual-V_{TH} assignment using the min-cut algorithm.

Implemented as a leakage-centric design-optimization methodology and flow, the min-cut approach generates a design with minimum leakage-power consumption. The right half of **Figure 2** depicts the flow. After the first optimization using the high-V_{TH} library, the design usually has timing violations. Incremental optimization using both low- and high-V_{TH} cell libraries identifies all timing-critical paths and replaces cells in these paths with low-V_{TH} cells. The synthesis tool also performs local design optimizations to fix timing violations in paths that still fail after low-V_{TH}-cell swapping.

Unlike the iterative min-cut algorithm, the iterative max-cut algorithm initially assigns all low-V_{TH} cells in a combinational circuit. Because low-V_{TH} cells are fast, this implementation meets the defined delay constraints with a positive margin but at the cost of high leakage-power consumption. Next, the algorithm identifies a maximum subset of edges, in which changing to high V_{TH} reduces leakage power without causing delay-constraint violations. The max-cut graph algorithm identifies these edges based on maximum-weight cut, which corresponds to the maximum-leakage-power reduction as the result of changing to high V_{TH}. The implementation of the algorithm, which the left half of **Figure 1** depicts, works in essentially the same way as the previous flow but with low- and high-V_{TH} libraries used in reverse order.

The third approach is a variation of the iterative max-cut algorithm (referred to as max-cut II) that improves on runtime and capacity. The max-cut II algorithm starts by assigning all high-V_{TH} cells to the design and then identifies critical subcircuits that violate timing constraints. All cells in the critical subcircuits are changed to low V_{TH} to meet the timing constraints. Next, the regular max-cut algorithm identifies edges that can tolerate a change back to high V_{TH} without causing delay violations. As a result, max-cut II essentially applies the max-cut algorithm only to critical subcircuits—greatly reducing the size of the optimized circuit.

This size reduction allows the flow implementation of the max-cut II algorithm to reduce chip area and optimization runtime compared with the regular max-cut approach (**Figure 3**). The max-cut II flow optimizes the design using the high-V_{TH} library for minimum leakage-power consumption. By lowering the clock frequency, however, you get an optimization with relaxed timing constraints to avoid working on timing-critical paths that cannot meet timing with only high-V_{TH} cells. After this initial optimization, you adjust the clock frequency up to its true target value to restore the actual timing constraints and then incrementally optimize the design using both low- and high-V_{TH} libraries.

POWER GATING

In standby mode, your design continues to consume leakage power—whatever amount you achieved with one of these optimization methods. One way to reduce leakage-power consumption in standby mode is to shut off the power supply to sections of logic. Because you can power down some logic while keeping other logic active, you must partition the design into two or more power islands. Then, you can gate the power to the appropriate islands for powering down.

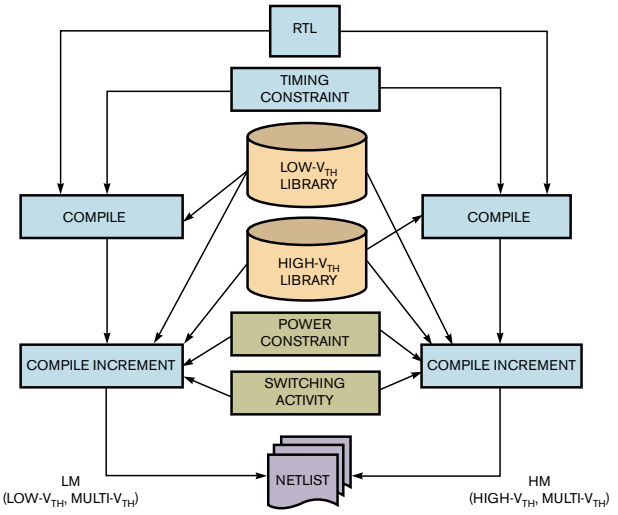

Figure 2 The options for the min- and max-cut flows appear on this flow chart's right and left sides, respectively. The only difference is that one begins with minimum leakage (high-V_{TH} cells) and the other begins with minimum delay (low-V_{TH} cells).

Although this power-gating approach achieves ultralow leakage power, the necessary methodologies are complex. They require the following special tasks in a design flow:

- Adding sleep transistors to shut off power supplies to idle circuits;
- Distributing power-gating control signals;
- Synthesizing power-island-aware clock trees;
- Retaining states of a subdesign in power-down periods;
- Isolating power-island interface signals; and
- Optimizing the multi-power-island physical design.

You can implement sleep transistors in a power-gating design based on gates, clusters, or power domains. In the gate-based implementation, you insert the sleep transistors into a logic gate to control power supplies to the gate. This approach offers the advantage that each gate can have the optimal-sized sleep transistor based on the gate's switching current and power-noise margin. Additionally, the virtual power nets are short and hidden in the gate, and you can implement the gates using standard-cell-based synthesis and physical-design tools. On the other hand, every gate has a sleep transistor, which increases area more than the cluster- and power-domain-based implementations. Distributing the global sleep-control signal to every gate is challenging in physical design.

In the cluster-based sleep-transistor implementation, you group the gates of a design into clusters. Choose a minimal number of clusters and minimal simultaneous switching current. The gates in a cluster belong to the same power domain and are close to each other in the layout. Each cluster connects to a virtual power net through a sleep transistor. The cluster-based implementation usually requires less area than the gate-based implementation, but obtaining realistic current estimates for each cluster to enable accurate sleep-transistor sizing is difficult. Moreover, the IR-drop variations among these individually powered

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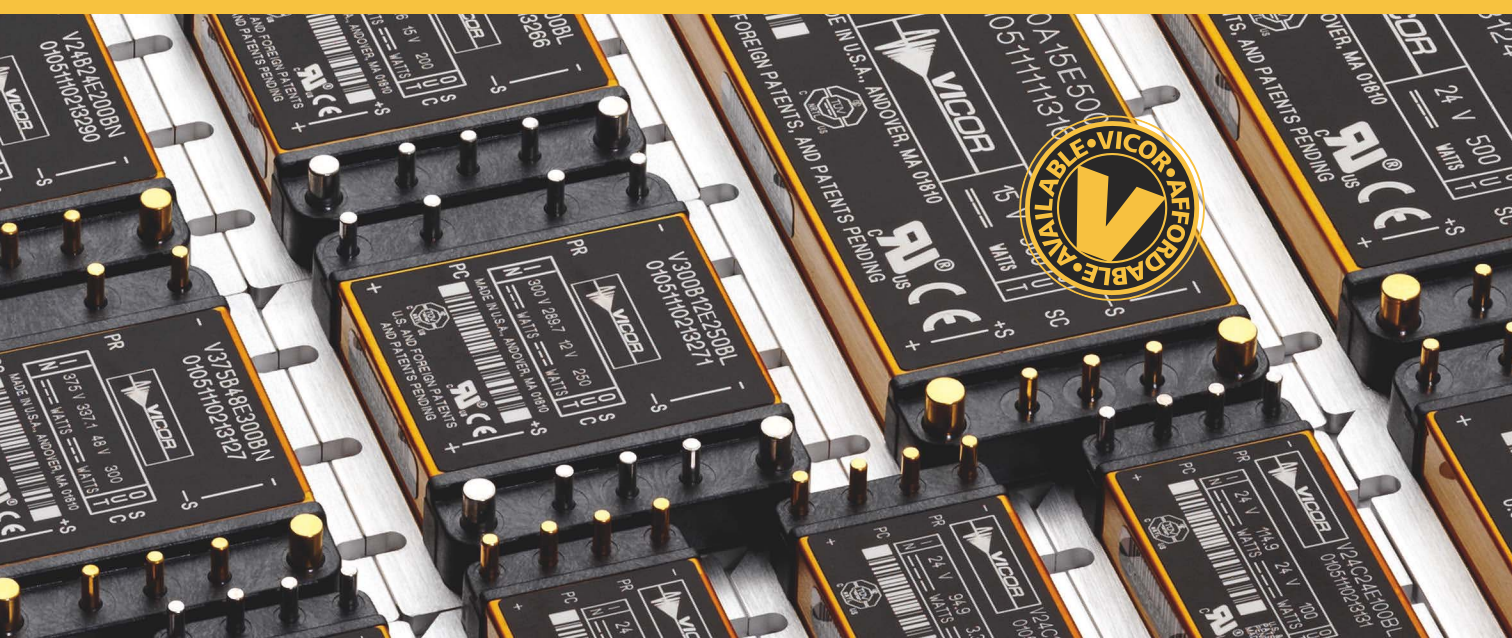

clusters result in performance variations.

In the power-domain-based sleep-transistor implementation, you connect gates in a power domain to a virtual power network that connects to a real power network through a number of sleep transistors. You can optimize the virtual power network in the same way as the real power network using normal power planning, analysis, and optimization methods. This sleep-transistor implementation usually requires less area than the gate- and cluster-based implementations because all gates in a power domain receive power via the distributed-sleep-transistor network in which the transistors share and balance the current discharge. Be aware that the virtual ground net tends to reduce the design's noise margin and can cause functional failure, so you have to carefully analyze the power needs of a power-gating design to ensure power integrity.

Whatever sleep-transistor approach you use, take care in routing the power-gating control signals to the transistors so that powering down a power island does not block the control-signal propagation to other power islands. A special buffer-tree-generation method can constrain creation and placement to ensure buffers are under the always-on power and ground nets. For similar reasons, constrain clock-tree synthesis to ensure that no clock branch passes through a power island, the shutdown of which would prevent the clock from getting to downstream logic.

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STATE RETENTION AND RESTORATION

Designs that resume operation after wake-up need a method for saving a power island's logic state before going idle and restoring the state at wake-up. You can choose among three types of state-retention and -restoration methods.

The first method relies on application software that writes specified register and memory values to disk storage before shutting down power supplies. At wake-up, the software writes the saved states back into the design. Although this method requires no special hardware design, the retention and restoration processes usually take too long to be useful in real applications. Moreover, the disk reads and writes consume a lot of power—possibly enough to cancel the leakage-power savings of short-term standby.

The second state-retention and -restoration method uses a design's scan chains to shift out register states into an always-powered memory before power-down and shift-in of the states at wake-up. Although much faster that the first method, this second method is still too slow for many leading-edge applications, and memory access still consumes too much power.

In the third method, you implement retention registers and latches that can efficiently store and restore states. Among the various types of retention circuits is the balloon-style circuit that is common in low-power designs. To implement such a circuit, you add a shadow latch to a normal register or a latch to save the register's state in power-down. The shadow latch comprises high-V_{TH} transistors for low leakage and connects to the normal register or latch through a single point like a tied balloon.

The balloon-style retention circuit introduces two retention-control signals, B1 and B2. You need to distribute these global signals in a similar way to the power-gating control signal to ensure valid signals at the retention circuits when you power down a power island in the signal path.

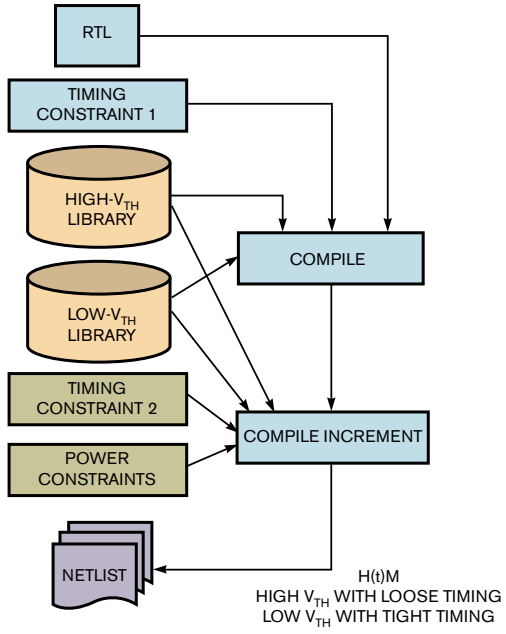


Figure 3 The max-cut II approach is the same as the max-cut flow in Figure 2, but it modifies only critical subcircuits. This approach reduces tool runtime.

ISLAND ISOLATION

When a power island powers down, its output signals float. These floating signals can affect other parts of the design that remain active. In the case of a handshake signal, a malfunction may occur. In any case, a floating signal may cause large short-circuit current in a receiving logic gate, resulting in wasted power and even device damage.

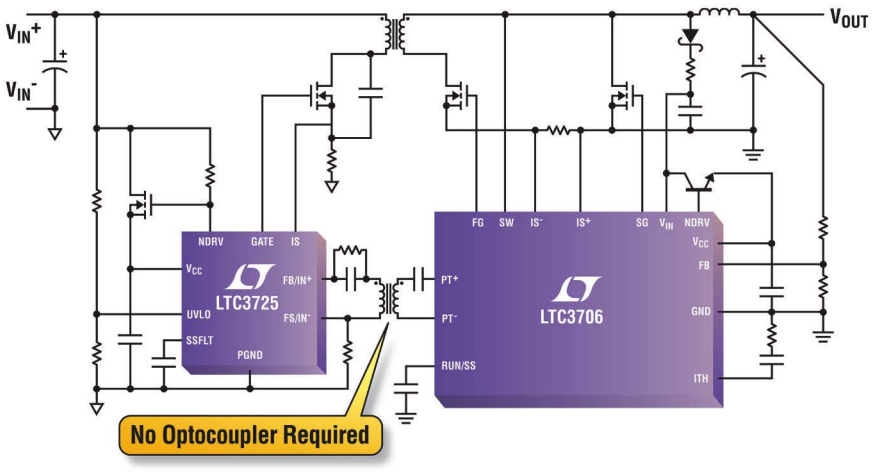
To avoid these problems, you need to add isolation logic at the interfaces between power-down and active-power islands. You can implement this isolation logic either in a power-down island to control output signals or in an active-power island to control input signals.

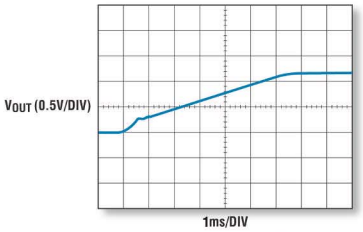
Isolating output signals usually requires fewer isolation cells than the input-signal-isolation method because outputs often drive multiple inputs of other power islands. Additionally, always-on power islands require no isolation cells at their outputs. Distribution of the output isolation control signal is also simpler.

On the other hand, output-signal isolation cells usually consume more power in standby mode because they must drive a large signal net, in contrast to the short local nets needed for input isolation cells. Moreover, you can implement the input-signal isolation logic with standard cells, but the output-signal isolation must rely on custom cells.

The choice of methods also depends on a design's power-management structure. For a design with one or two gating power islands, an input-signal-isolation method usually makes the best

Think Outside the Brick





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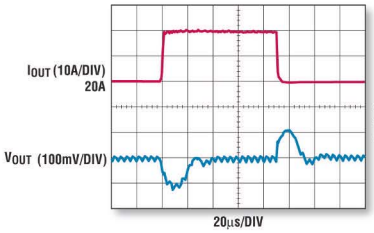

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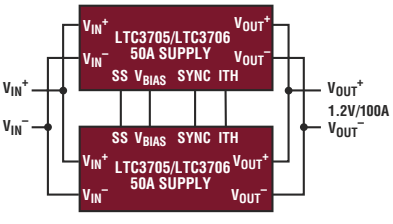

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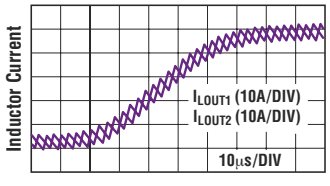

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sense. For designs with more complex power-management structures, the output-signal-isolation method is usually a better choice.

Various combinations of gates and transistors are suitable for achieving the necessary pullup or pulldown state under control of the power-gating signal. During placement and physical synthesis, make sure that the input isolation cells are inside the power island and close to the power-island boundary. And check the results of physical synthesis to make sure that the tool never inserts a buffer between the isolation cells and the inputs of a power island. Any such buffer defies the purpose of isolation cells.

POWER-ISLAND-AWARE DESIGN OPTIMIZATION

Sleep transistors, state-retention cells, and interface-signal isolations make design optimization a complex task. These guidelines can help achieve good results:

- Use strict exclusive region constraints during placement and physical synthesis to ensure that cells in a power island are placed inside the island. This placement also requires design specifications of logical hierarchy in association with the power island.
- Assign new cells created during restructuring logic or local buffering in a power island to the power island and apply constraints to ensure that they are inside the power island.
- Place all special cells that require always-on power supplies, such as state-retention cells, under always-on power and ground nets. Some tools automatically handle this task.
- Place a power island's signal-isolation cells at the island's boundary to ensure that cross-power-island signals are isolated.
- Create global signal distributions and manage scan-chain stitching so that powering down a power island does not block signals or scan chains in the rest of the design.

Applying all of these constraints increases runtime, so implementing power-down islands is a useful strategy only for applications that demand the lowest possible leakage-power consumption. For most designs, the automated dual-V_{TH} methodologies provide good results with little effort. EDN

AUTHOR'S BIOGRAPHY

Kaijian Shi is a principal consultant with Synopsys Professional Services. He holds a bachelor's degree in physics, master's degree in computer science (Shanghai Teachers University, China), master's degree in electrical engineering (University of Birmingham, Birmingham, UK), and doctorate in electrical engineering (University of Kent, Canterbury, UK). Shi has served or is currently serving as chairman of the IEEE Dallas Section (2006), chairman of the IEEE Circuits and System Society Dallas Chapter (2004), track chairman of the IEEE SOC Conference (2005, 2006), track organizer of IEC DesignCon (2003 to 2006), and member of the technical-program committees of IEEE ASP-DAC (2005) and IEEE ISVLSI (2006). He has published nine journals and 33 international-conference papers.

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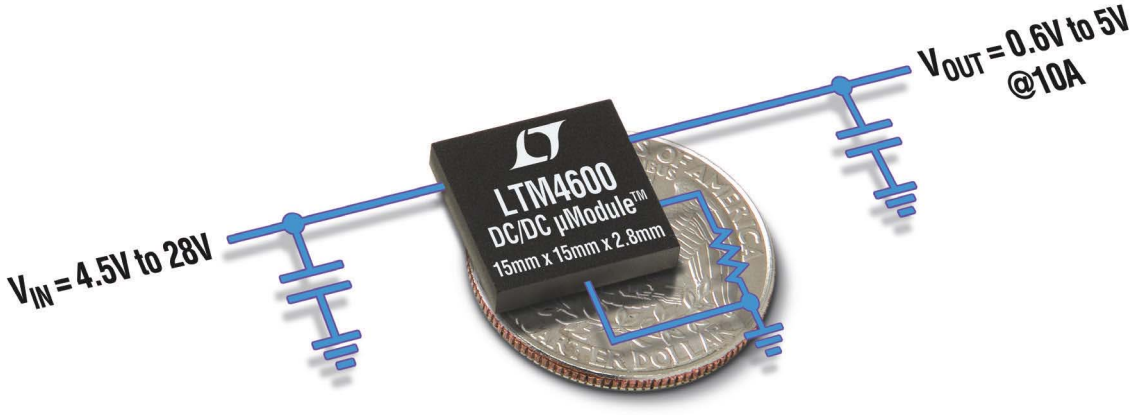

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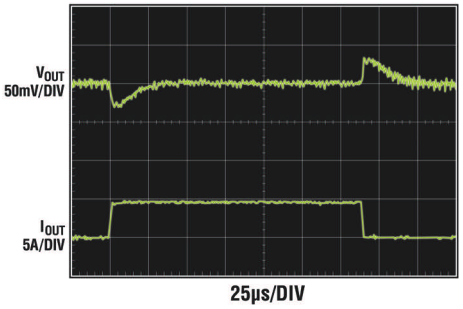

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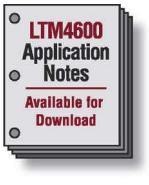

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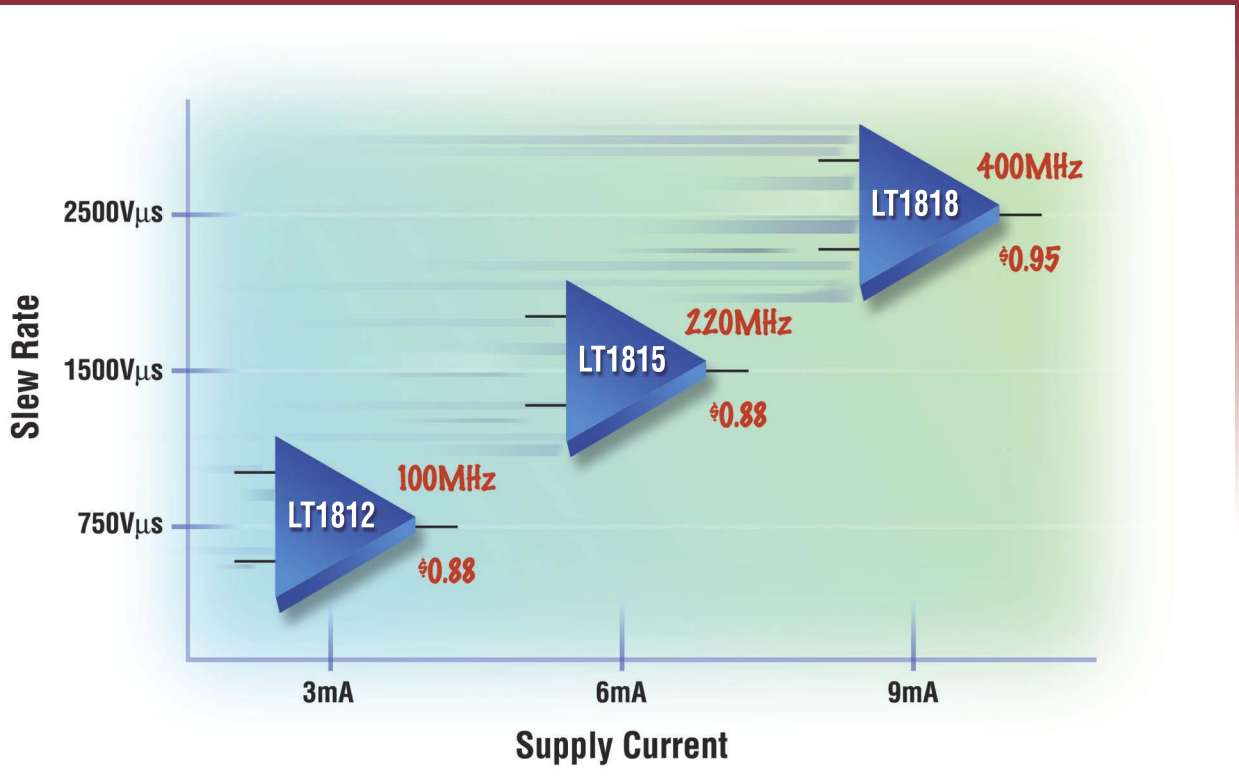

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DESIGN NOTES

Baseband Circuits for an RFID Receiver – Design Note 381

Philip Karantzalis

Introduction

Radio Frequency Identification (RFID) technology uses radiated and reflected RF power to identify and track a variety of objects. A typical RFID system consists of a reader and a transponder (or tag). An RFID reader contains an RF transmitter, one or more antennas and an RF receiver. An RFID tag is simply an uniquely identified IC with an antenna.

Communication between a reader and a tag is via backscatter reflection, similar to a radar system, in the UHF frequencies from 860MHz to 960MHz. This design note describes a high performance RFID receiver.

A Direct Conversion Receiver

Figure 1 shows the block diagram of a direct conversion RF receiver—the receiver demodulates an RF carrier directly into a baseband signal without an intermediate frequency down-conversion (a zero IF receiver).

The antenna, shared by both the transmitter and receiver, detects an RF carrier and passes it through a bandpass filter to an LT®5516 demodulator's RF input.

The LT5516 direct conversion demodulator frequency range of 800MHz to 1.5GHz includes the UHF range used by RFID readers (860MHz to 960MHz). The excellent linearity of the LT5516 provides for high sensitivity to low level signals, even in the presence of large interfering signals.

The LT6231 low noise dual op amp acts as a differential to single-ended amplifier to drive the single-ended input of the lowpass filter.

Analog baseband filtering is performed by the LT1568, a low noise, precision RC filter building block. The LT1568 filter provides a simple solution for designing lowpass and bandpass filters with cutoff frequencies from 100kHz to 10MHz. These cutoff frequencies are sufficient for the 250kHz to 4MHz signal spectrum typically used in UHF RFID systems.

The differential output of an LT1568 drives the inputs of an LTC2298 ADC. The LTC2298 is a 65Msps, low power (400mW), dual 14-bit analog to digital converter with 74dB signal-to-noise ratio (SNR). The digital signal processor (DSP) that follows the ADC analyzes the received signal from multiple tags and provides additional filtering.

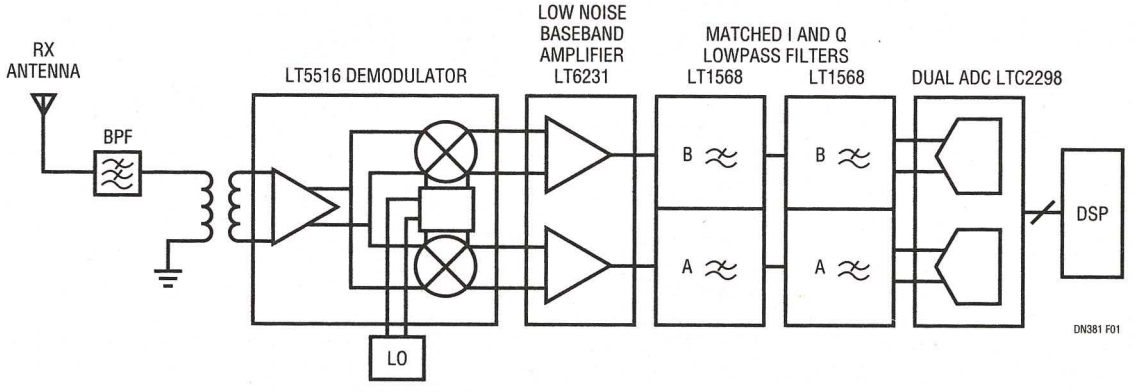

Figure 1. A Direct Conversion Receiver for an RFID Reader

A Low Noise Differential to Single-Ended Amplifier

Figure 2 shows an LT6231 difference amplifier used to convert the LT5516 differential I or Q output to a single-ended output. The addition of external 270pF capacitors across the 60Ω resistors limits the demodulator's output to 10MHz to prevent any high frequency interference from reaching the LT6231 amplifier.

AC coupling to the baseband amplifier is used because DC coupling is not necessary for the amplitude shift keying (ASK) RFID signal.

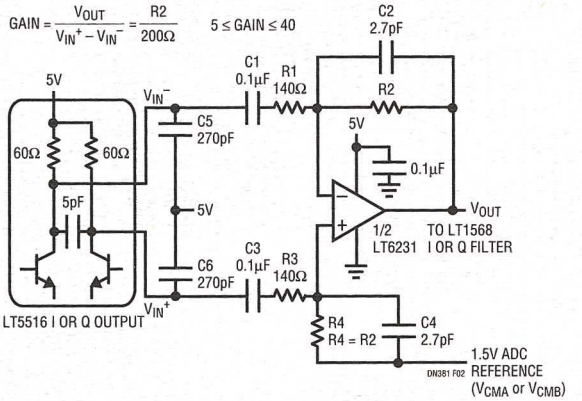

Figure 2. A Low Noise I or Q Baseband Interface

The highpass pole provided by the AC coupling capacitors and the amplifier input resistors is set to 8kHz. The differential amplifier's input resistors are set to 140Ω in order to minimize the input referred noise. The noise floor at the amplifier's output is 4.3nV/√Hz times the amplifier gain (gain ≥ 5). The 1.5V reference provided by the LTC2298 ADC is used to level shift the amplifier's output to the mid-supply point of the following 3V filter and ADC circuits.

A Matched I and Q Filter and a Dual ADC

Figure 3 shows two LT1568 filter building blocks connected as dual, matched, fourth order filters. The LT1568 filter's single-ended input to differential output conversion gain is 6dB. The LT1568 circuit implements an elliptic lowpass filter function with equal resistor values (see Figure 3). Stopband attenuation at $2(f_{-3dB})$ is 34dB. I and Q filter matching is assured by the inherent matching of the LT1568s' A and B sides.

The input voltage range of an LTC2298 is adjustable to $2V_{P-P}$ or $1V_{P-P}$.

Conclusion

Using only five ICs (LT5516, LT6231, two LT1568 and an LTC2268), a high performance UHF RFID receiver can be designed with the flexibility to adapt and be optimized to meet the requirements of the present and emerging RFID standards.

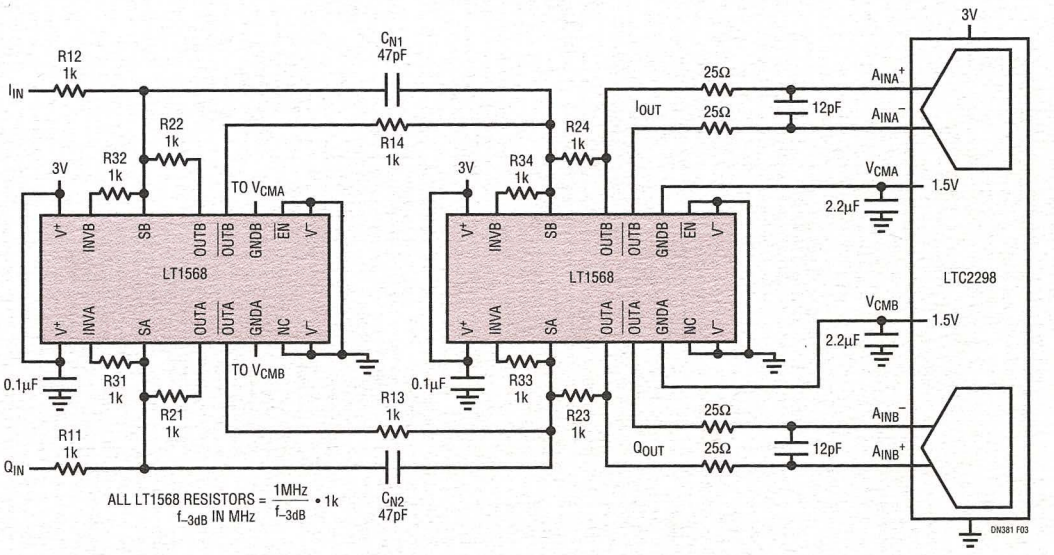

Figure 3. A Matched, 1MHz, 4th Order, I and Q Lowpass Filter and ADC Driver

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READERS SOLVE DESIGN PROBLEMS

Hardened Ethernet cable goes underground

Philip Freidin, Fliptronics, Sunnyvale, CA

An application required the extension of Ethernet (IEEE 802.3u-1995) service from a home to a garage, a distance of approximately 300 ft. Wireless communication using IEEE 802.11a/b/g equipment had proved unreliable due to the buildings' construction, which comprises stucco over embedded wire mesh. In effect, the buildings' walls form Faraday cages that attenuate radiated signals. Straight-line aerial deployment of the Ethernet cable between buildings would have required installation of support poles, and simply laying the cable on the surface of the ground would expose the cable to damage from automobiles, hungry pets, and inquisitive children. At first glance, burial of the cable appeared impractical due to the presence of a large concrete surface between the buildings. However, an alternate route through an adjacent garden would avoid tunneling beneath the concrete slab but would expose the cable to environmental hazards, such as spade work and burrowing animals.

This Design Idea describes how to environmentally "harden" a Category 5 UTP (unshielded-twisted-pair) cable conforming to EIA/TIA 568B and ISO/IEC 11801:1995 that's terminated with RJ-45 connectors (ISO 8877). Without adding repeaters, a Category 5 Ethernet cable can extend to 100m, or a little more than 300 ft. In this application, the cable run comprises 100 ft of exposed cable, 100 ft of "garden-grade" protected cable, and 100 ft more of exposed cable. To apply the idea, you have to find a way to protect and handle the exposed 200 ft of cable.

Depending on your installation's requirements, you will need various numbers and lengths of the following parts: a 100-ft-long garden hose whose fittings conform to the ANSI/ASME B1.20.7-1991.75-11.5 NH thread-form standard; a 4-Gbyte SCSI disk drive, which need not be functional; a continuous, 300-ft-long Category 5 Ethernet cable terminated in RJ-45 connectors; a 120-ft-long, nylon twine; a 5-in.-long, electrical-grade, adhesive-backed tape; a 2-in.-steel, socket-head-cap, 1/4-20-thread machine screw (ANSI/ASME B1.1-1989); and two bricks.

To construct the design, uncoil and stretch the garden hose as straight as possible, perhaps using a driveway as a work surface. Place a brick on each end of the hose to prevent it from curling. If you use only one length of garden hose, cut off and discard the hose fittings. Using Torx or Philips screwdrivers as appropriate, dismantle the 4-Gbyte SCSI disk drive by removing all of the screws that retain the drive's cover. If the cover resists removal, look for screws beneath labels. Remove the drive's head-positioning magnets, which can exert a strong pull on nearby ferrous objects. Use caution to avoid pinching your fingers between the magnets and the steel surfaces. Discard the remainder of the SCSI drive.

Securely tie the nylon twine to the 1/4-20 steel machine screw and insert the screw into one end of the hose. Apply the magnet to the hose's exterior to attract the machine screw. Slide the magnet along the hose to pull the nylon twine through the hose. When the screw reaches the hose's far end, untie the twine and save the screw for future use. To ease manipulation of the Category 5 cable, deploy it from either its original dispenser box or a spool mounted on a suitable axle so that the cable can easily unwind. Securely attach the twine to one end of the Category 5 cable. Walk to the far end of the hose and gently pull the cable through the hose. If you encounter excessive resistance, investigate the cause and remove any cable kinks or feeder-end snags.

When the cable appears at the pulling end, stop for a moment. Go to the other end of the hose and wrap an inch or two of electrical tape around the cable where it's just about to enter the hose. Return to the far end of the hose and continue pulling the cable through the hose. Stop pulling when you see the electrical-tape marker. You now have a 300-ft-long Category 5 cable whose central 100 feet the garden hose protects. If you decide to protect more of the cable, repeat the process by feeding the twine through a second length of hose. Use the hoses' couplings to make a watertight joint between lengths. If you take this approach, make sure that you properly orient the hose segments before you spend too much time threading the twine through the hose. EDN

DIs Inside

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Shunt regulator improves power amplifier's current-limit accuracy

John Guy, Maxim Integrated Products Inc, Sunnyvale, CA

Adding current-limiting circuitry to a power amplifier's or a linear voltage regulator's emitter-follower output stage protects both the output transistor and the downstream circuitry from excessive-current damage. **Figure 1** shows the classic current-limiter circuit: Transistor Q_2 senses the output-current-induced voltage drop across ballast resistor R_2 and diverts base current from Darlington-connected transistors Q_1 and Q_3. Transistor Q_2's base-emitter voltage, V_{BE}, sets the circuit's current-limit threshold. Unfortunately, a small-signal transistor's V_{BE} exhibits a temperature coefficient of −2 mV/°C, which causes a substantial variation in the current-limiting threshold over the circuit's operating-temperature range.

You can improve the circuit's performance by replacing Q_2 with IC_1, an adjustable shunt regulator (**Figure 2**). With an input threshold voltage of 0.6V, the MAX8515 allows use of a lower value for current-sense resistor R_2 and thus helps minimize R_2's power and thermal losses. Alternative commonly available shunt regulators present input voltages of 1.25 to 2.5V. In addition, a separate power-supply input connection allows the MAX8515 to maintain accuracy when its internal output transistor approaches saturation.

Figure 3 compares current-limit accuracy for the circuits of **Figure 1** and **Figure 2** over an operating-temperature range of −40 to +85°C. Neglecting the temperature coefficient of sense resistor R_2, the shunt-regulator version maintains its output current to an accuracy of better than 2%, and the small-signal-transistor version exhibits a 25% current variation over the operating-temperature range. EDN

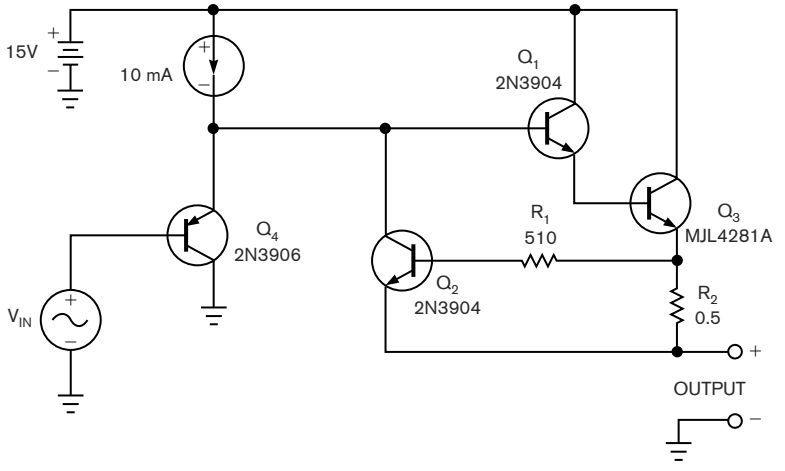

Figure 1 A small-signal transistor, Q_2, provides an output-current limit for this emitter-follower power amplifier.

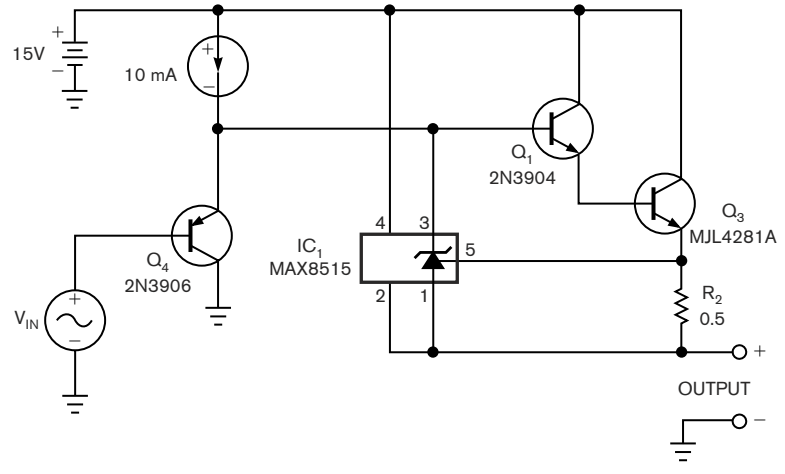

Figure 2 Substituting a shunt regulator, IC_1, for Q_2 in Figure 1 improves the output-current-limit accuracy.

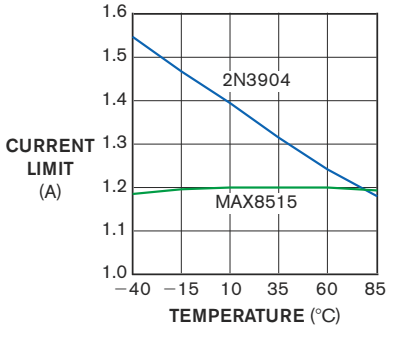

Figure 3 Output-current-versus-temperature plots for the circuits of figures 1 and 2 show improved accuracy for the shunt-regulated circuit (bottom trace) over the discrete-transistor version (top trace).

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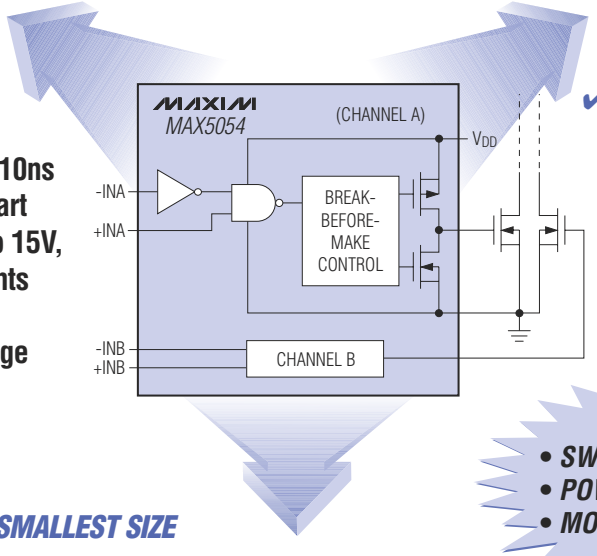

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Low-power, super-regenerative receiver targets 433-MHz ISM band

Cedric Mélange, Johan Bauwelinck, and Jan Vandewege,
Ghent University, Ghent, Belgium

Designers often choose a super-regenerative receiver—despite its frequency instability and poor selectivity—for battery-powered, short-range, wireless applications in which power consumption is a major issue. Examples include remote-keyless-access systems, automobile alarms, biomedical monitors, sensor networks, and computer peripherals (**Reference 1**). A super-regenerative detector can also demodulate frequency-modulated signals through slope detection. Tune the detector so that the signal falls on the slope of the detector circuit's selectivity curve. This Design Idea presents a super-regenerative receiver that consumes less than 1 mW and operates in the license-free, 433-MHz ISM (industrial/scientific/medical) band.

In its simplest form, a super-regenerative receiver comprises an RF oscillator that a "quench signal," or lower frequency waveform, periodically switches on and off. When the quench signal switches on the oscillator, oscillations start to build up with an exponentially growing envelope. Applying an external signal at the oscillator's nominal frequency speeds the growth of the envelope of these oscillations. Thus, the duty cycle of the quenched oscillator's amplitude changes in proportion to the amplitude of the applied RF signal (**Figure 1**).

A super-regenerative detector can receive AM signals and is well-suited for detecting OOK (on/off-keyed) data signals. The super-regenerative detector constitutes a sampled-data system; that is, each quench period samples and amplifies the RF signal. To accurately reconstruct the original modulation, the quench generator must operate at a frequency a few times higher than the highest frequency in the original modulating signal. Adding an envelope detector followed by a lowpass filter improves AM demodulation (**Reference 2**).

IN ITS SIMPLEST FORM, A SUPER-REGENERATIVE RECEIVER COMPRISES AN RF OSCILLATOR THAT A "QUENCH SIGNAL," OR LOWER FREQUENCY WAVEFORM, PERIODICALLY SWITCHES ON AND OFF.

Figure 2 is a block diagram of the super-regenerative receiver circuit in **Figure 3**. The heart of the receiver comprises an ordinary Colpitts-configured LC oscillator operating at a frequency that the series resonance of L_1, L_2, C_1, C_2, and C_3 determines. Switching off transistor Q_1's bias current quenches the oscillator. (Note that increasing C_1 and C_2 improves the oscillator's frequency stability at the expense of increased power consumption.) Cascode-connected transistors Q_2 and Q_3 form an antenna amplifier that improves the receiver's noise figure and provides some RF isolation between the oscillator and the antenna. To conserve power, the amplifier operates only during oscillation growth.

Based on a Schmitt-trigger circuit, the quench generator switches the oscillator and RF-amplifier stage. To improve sensitivity, the triangular waveform across C_5 quenches the oscillator, and the square wave at the output of IC_1 switches the RF amplifier. The quench generator's two outputs are phased in quadrature so that the RF amplifier has received power when the detector's oscillations start to grow. The quench frequency of this circuit is 100 kHz to allow data transfers at rates as high as 20 kbps.

The envelope detector comprises a common-source amplifier that's nominally biased to operate in Class B mode. To increase this stage's gain, you apply a small amount of bias current to make it operate in Class AB mode. To reduce the load on the oscillator's LC tank circuit, C_{10} connects to a tap on inductor L_1, as inductor L_2 shows.

The first stage in the data-recovery circuit comprises buffer IC_{2A}; amplifier IC_{2B}; and a third-order, lowpass filter for suppressing quench-frequency components in the envelope detector's output. A dc-coupled Schmitt-trigger circuit, IC_3, extracts the transmitted data from the demodulated signal. A lowpass filter comprising C_{12} and R_{16} extracts the demodulated signal's dc

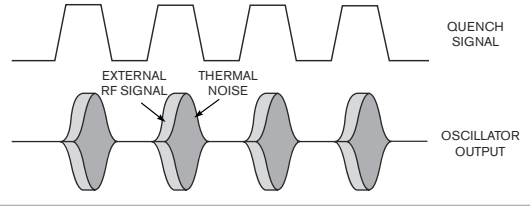

Figure 1 In a super-regenerative detector, the arrival of a signal starts RF oscillations sooner than under no-signal conditions.

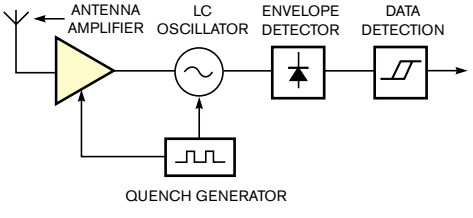

Figure 2 The super-regenerative receiver is considerably simpler than a superheterodyne circuit.

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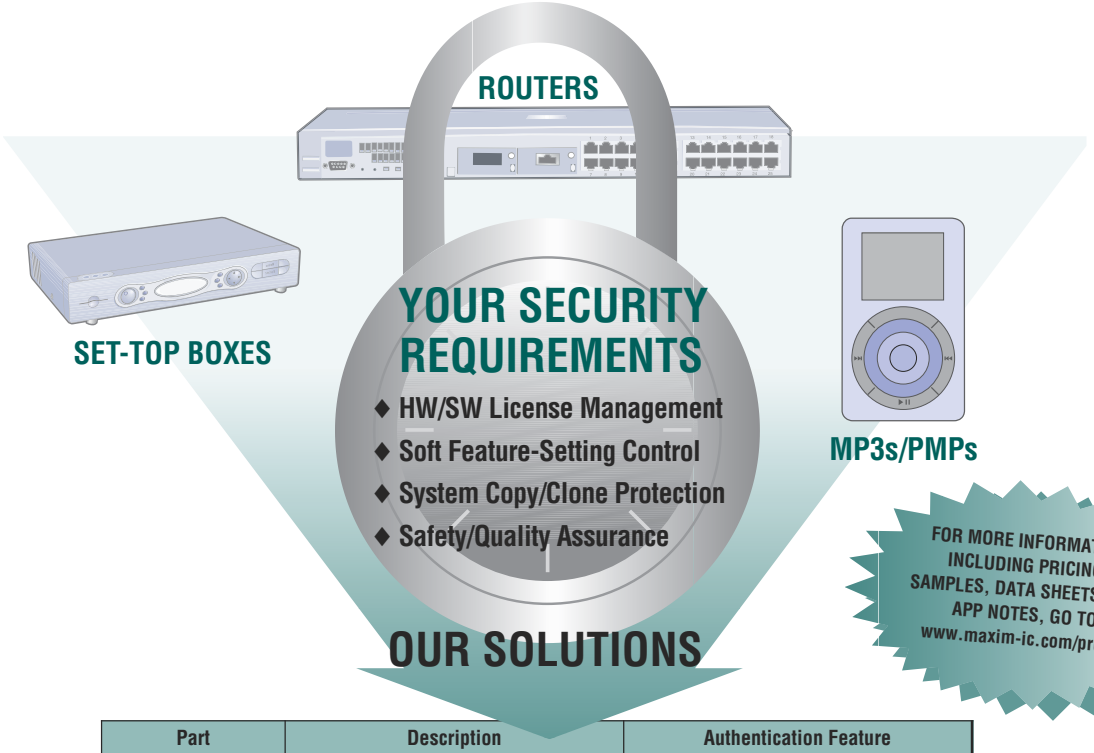

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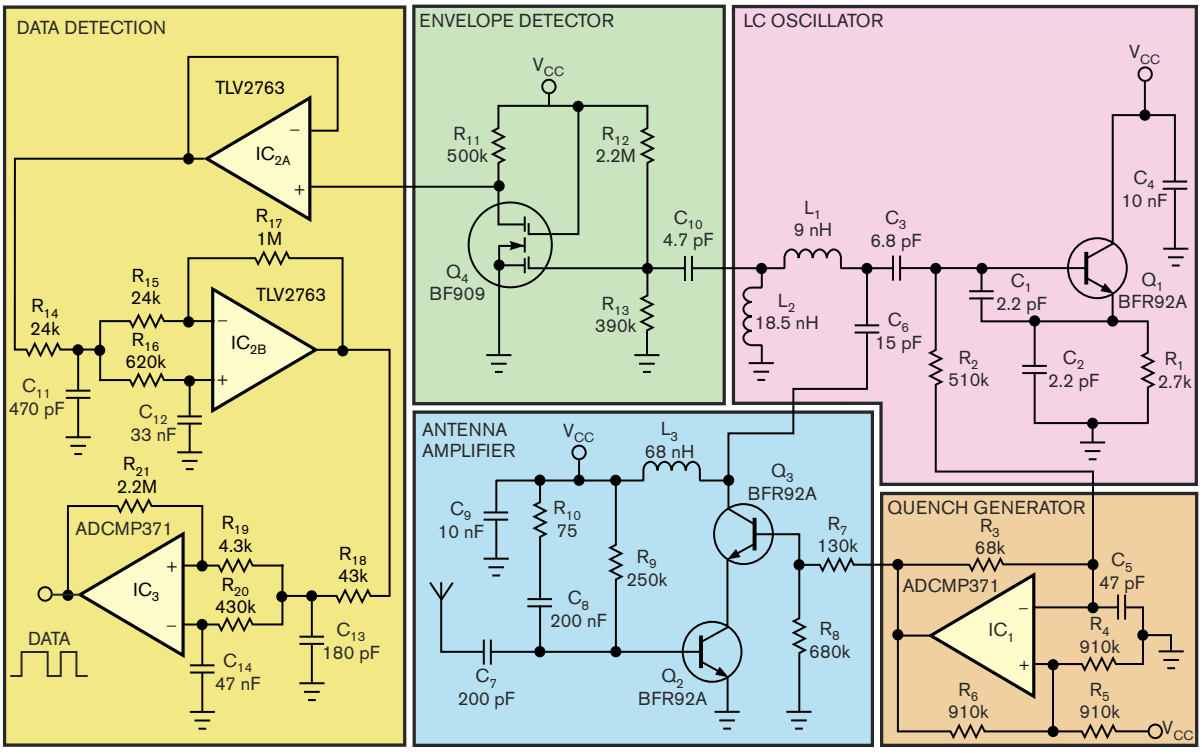

Figure 3 The super-regenerative receiver features relatively few components.

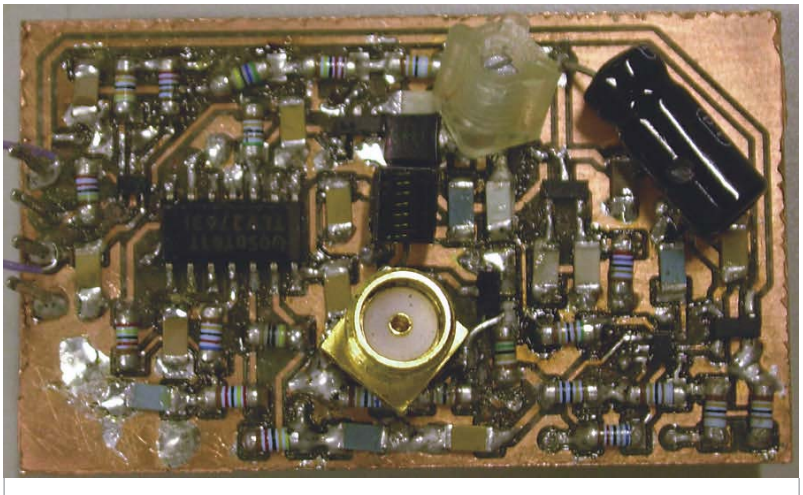

Figure 4 A prototype version of a super-regenerative receiver uses mostly surface-mount components. The large, black, leaded component in the upper right corner is a power-supply-decoupling capacitor. Note the RF-input connector in the center of the pc board.

component and sets the Schmitt trigger's decision threshold. As a consequence, the data transmitter must use a dc-balanced coding scheme, such as Manchester coding, for modulation. On the receiving end, no additional active components are necessary for extracting the data-recovery circuit's decision threshold, which helps minimize the receiver's power consumption.

The prototype occupies a compact pc board measuring approximately 5×3 cm (**Figure 4**). Using a simple, homemade PRBS (pseudorandom-binary-sequence) generator that uses Manchester coding with a 28-to-1-bit sequence (**Reference 3**), BER (bit-error-rate) measurements yield the results in **Figure 5**. These results demonstrate a sensitivity of less than −100 dBm for a 10-to-4 BER at 1 kbps. The receiver consumes 270 µA at 3V for a power consumption of 810 µW. As a further

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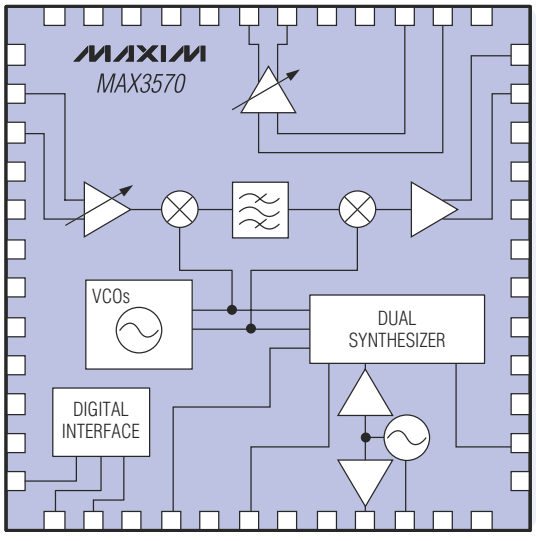

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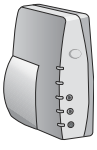

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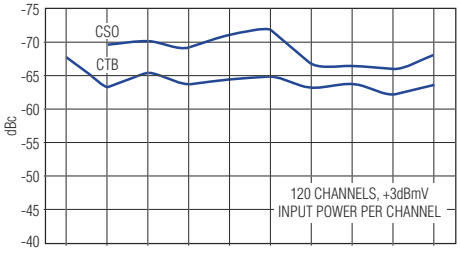

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enhancement to the design, it includes a transmitter circuit based on Maxim's MAX1472, creating a simple, compact, low-cost, and low-power transceiver for the 433-MHz ISM band. You can easily adapt the receiver circuit for recovery of AM audio or other analog signals by replacing the Schmitt trigger, IC_3, with a conventional audio-output amplifier. Retune the RF oscillator to cover the frequency range of interest. EDN

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3 Mélange, Cedric, Johan Bauwelinck, Jo Pletinckx, and Jan Vandewege, "Low-cost BER tester measures errors in low-data-rate applications," *EDN*, Dec 5, 2005, pg 123, www.edn.com/article/CA6288033.html.

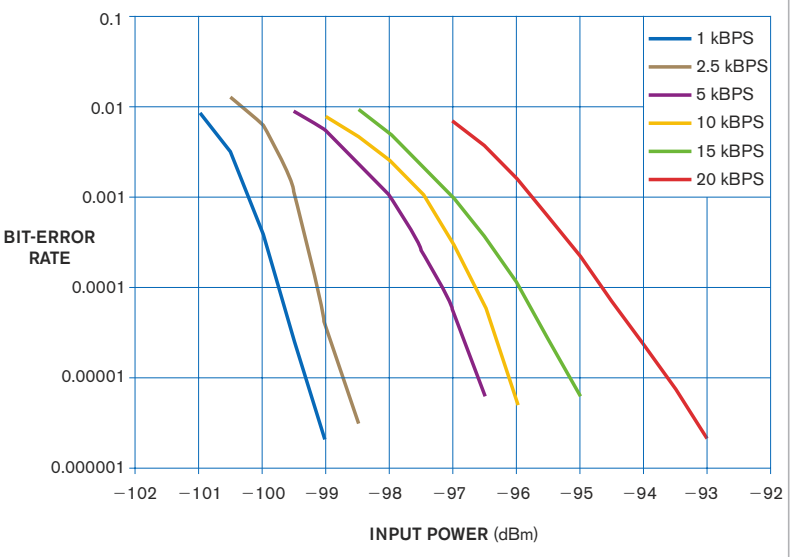
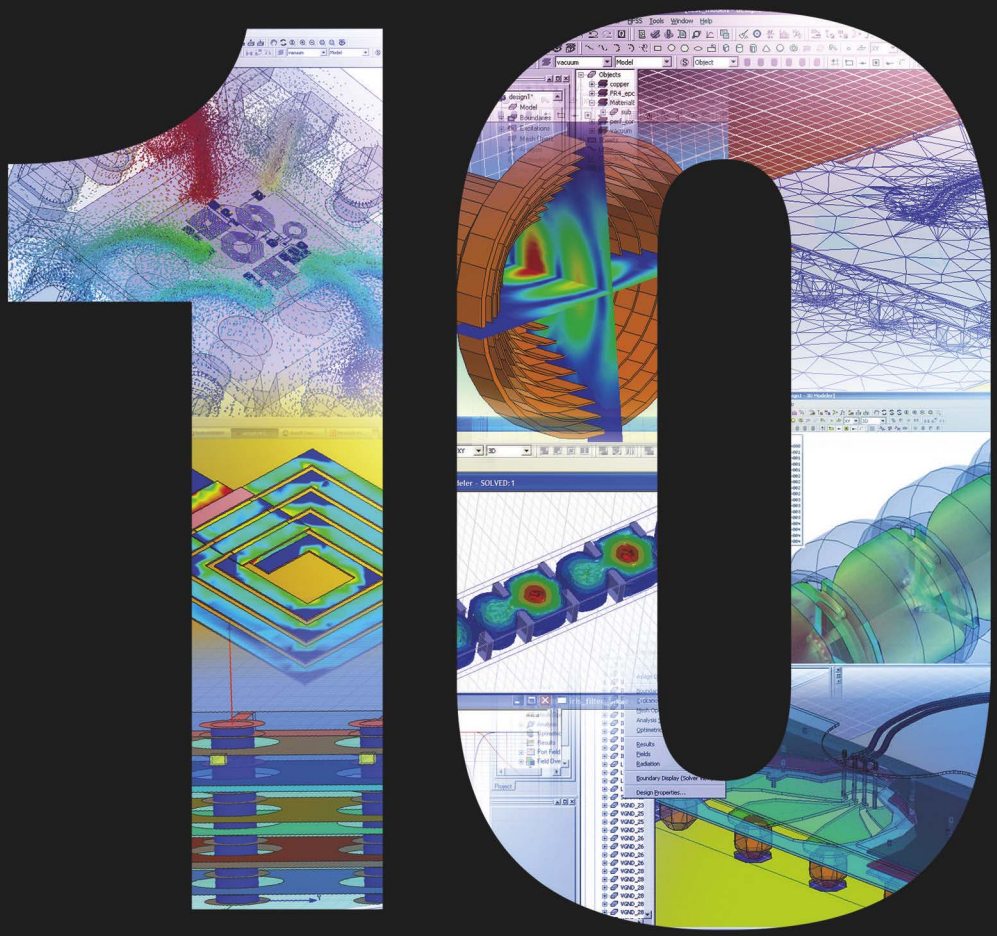


Figure 5 Measurements of bit-error rate versus input RF power highlight the prototype receiver's sensitivity. The frequency is 433.92 MHz.



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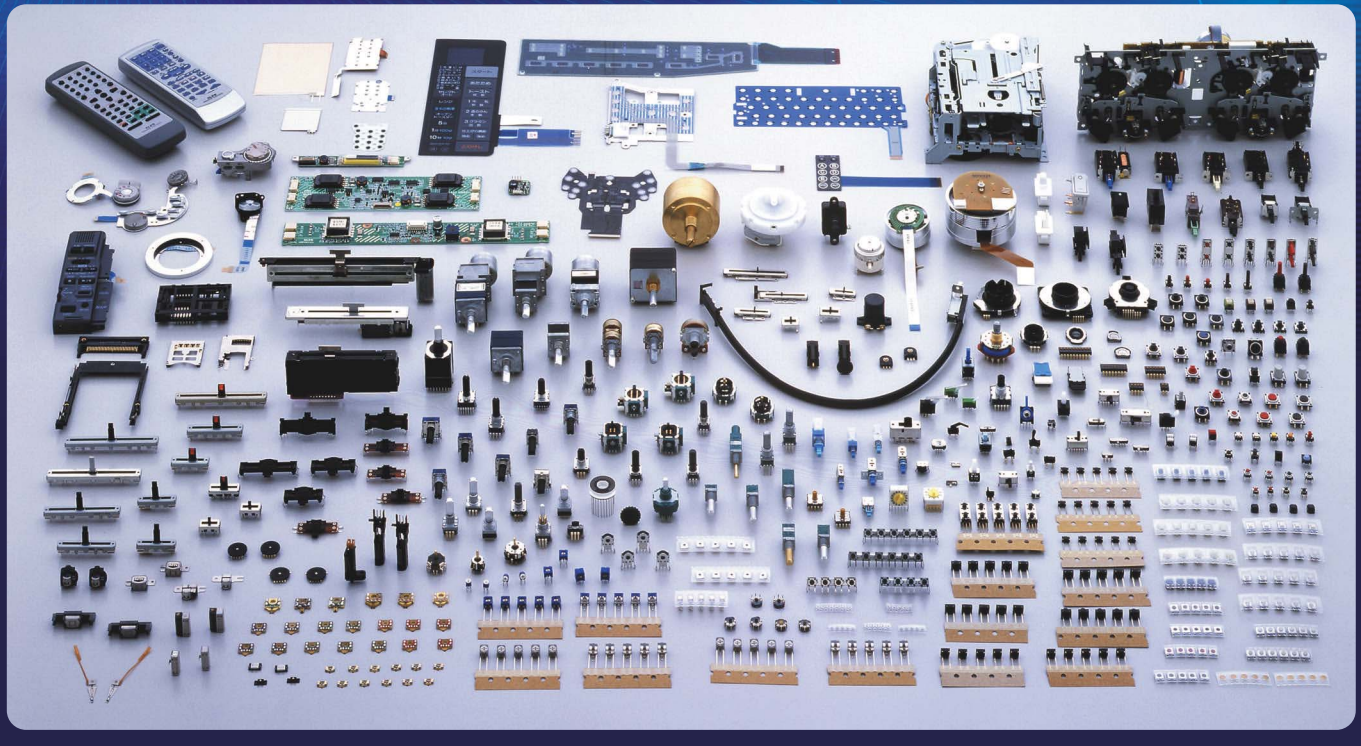

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California Micro Devices, www.calmicro.com

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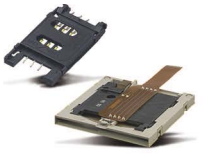

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